The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC871

One Socket PC Card Interface

Version 3.0

User Manual

Issue 1.2

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TPMC871-10

One socket PC Card with PMC front panel (inserted PC Card sticks out of the front panel)

TPMC871-11

One socket PC Card without PMC front panel (inserted PC Card is aligned with PMC board border)

TPMC871-50

One socket PC Card with PMC front panel, same as TPMC871-11 but with PMC front panel (inserted PC Card is located behind front panel)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue (Board version 3.0)	October 2003
1.1	Changed Configuration EEPROM	December 2003
1.2	New address TEWS LLC	September 2006

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1 Product Description

The TPMC871 is a standard single-width 32 bit PMC module with one interface for 16 bit PC Card or 32 bit CardBus cards using the PCI1510 PC Card controller and a power management unit. The register map of the PCI1510 PC Card controller is Intel 82365-DF compatible.

The power management unit provides 3.3V or 5.0V PC Card power supply and 3.3V, 5.0V or 12V PC Card programming voltage. Due to the short circuit and thermal protection of the power management unit no external fuses are needed on the module.

The TPMC871 Version 3.0 is in PC Card 16 mode functional fully compatible to its predecessors, the TPMC871 Version 1.0 and Version 2.0.

The TPMC871 with the PC Card socket controller PCI1510 provides full ExCA register implementation of one 16 bit PC Card compatible with PCMCIA 2.1/JEIDA 4.2 standards. Both memory and I/O cards are supported. Up to five memory windows and up to two I/O windows are available for PC Card 16 accesses. For 32 bit CardBus Cards two memory windows and two I/O windows are supported by the PCI1510 controller. CardBus Card status information can be accessed in five CardBus socket registers which can be mapped in the host memory space.

The PC Card assembly has a maximum component height of 5.6mm which is 0.9mm above the specified component height (4.7mm) according to IEEE1386.1. The TPMC871 Version 3.0 will power up in the 16 bit PC Card mode.

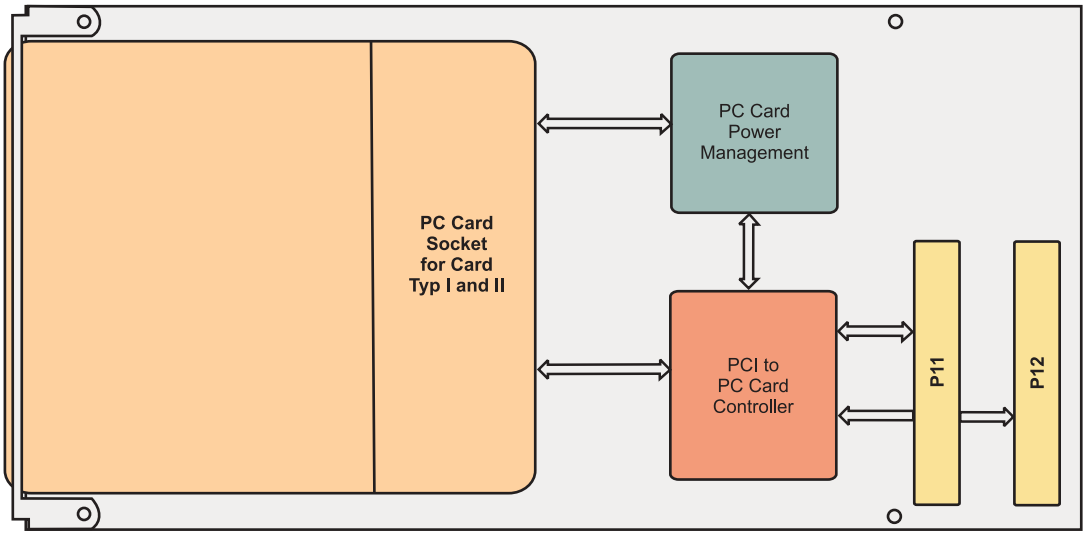

Figure 1-1 : Block Diagram TPMC871

1.1 Module TPMC871-10

The inserted PC Card sticks out of the PMC front panel.

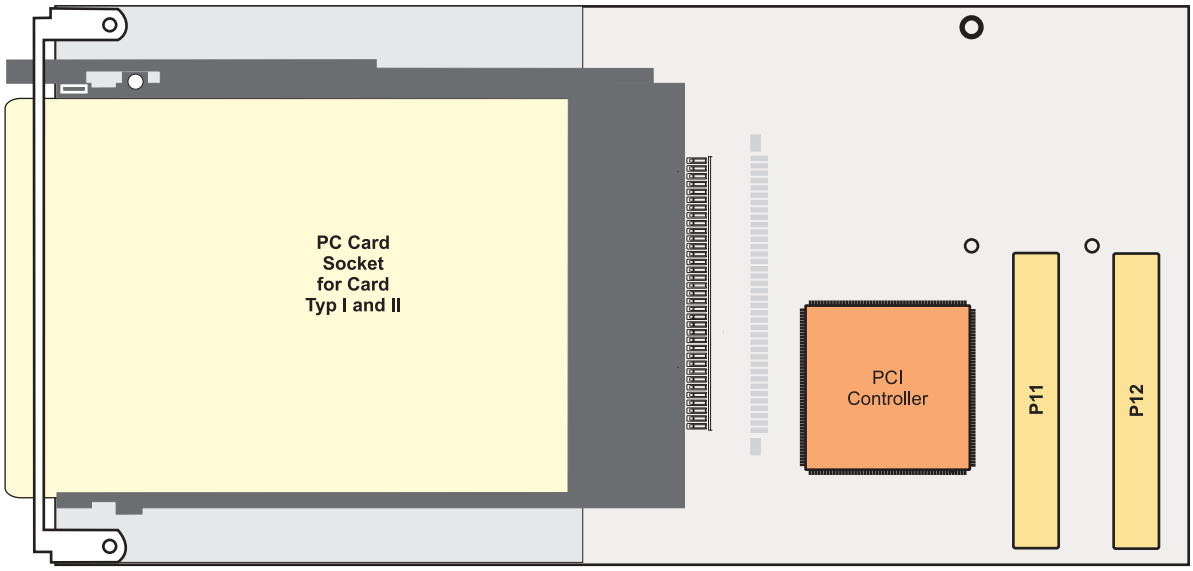

Figure 1-2 : Module TPMC871-10

1.2 Module TPMC871-11

The PC Card is aligned with the border of the PMC board. The TPMC871-11 has no front panel.

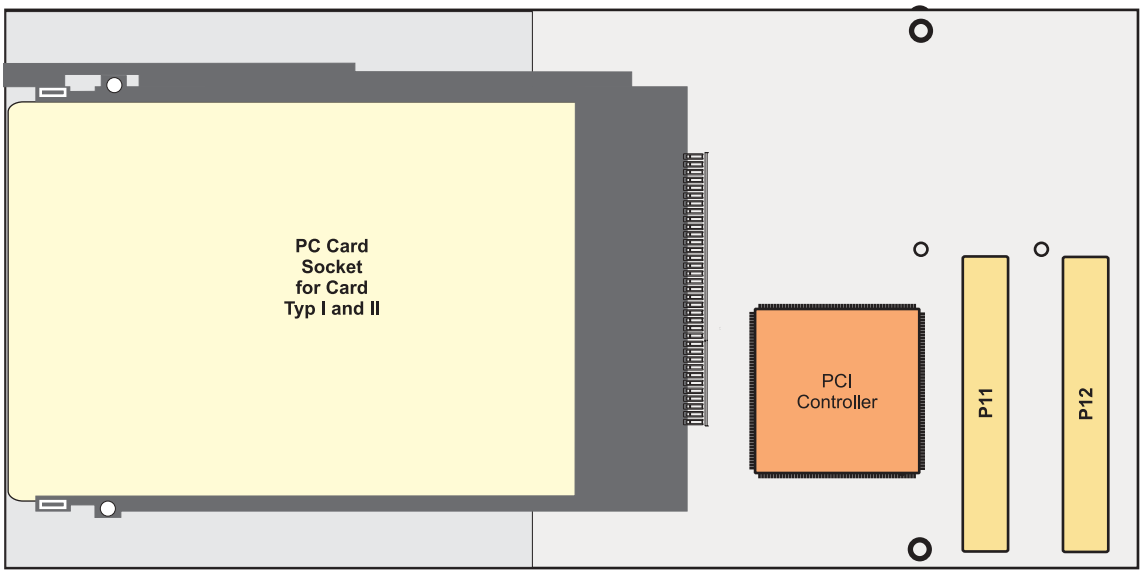

Figure 1-3 : Module TPMC871-11

1.3 Module TPMC871-50

The TPMC871-50 is the same module as TPMC871-11 but it has a PMC front panel. The inserted PC Card is located behind the front panel.

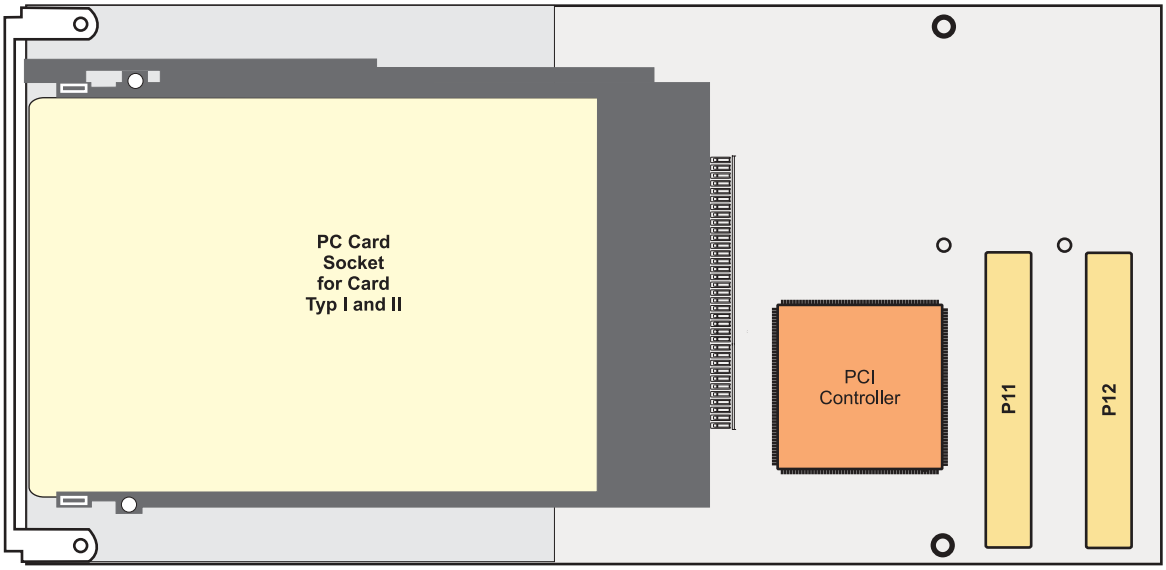

Figure 1-4 : Module TPMC871-50

2 Technical Specification

Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Controller	Texas Instruments PCI1510	
CMC Module	PMC module conforming to IEEEP1386.1 **The PC Card assembly has a maximum component height of 5.6mm which is 0.9mm above the specified component height (4.7mm) according to IEEE1386.1.**	
Module Specific Data		
PC Card Interface	16 bit PC Card electrical interface 32 bit CardBus electrical interface	
PC Card Slot	1 socket for card types I and II	
PC Card Operating Voltage	+3.3V or +5V	
PC Card Programming Voltage	+3.3V/+5V or +12V	
PC Card Supply Current	1A maximum	
PC Card Programming Current	150mA maximum	
Physical Data		
Power Requirements	70mA typical @ +3.3V DC 5mA typical @ +5V DC <2mA typical @ V(I/O)	
Power Requirements with PC Card	Voltage and current depends on the used PC Card	
Temperature Range	Operating Storage	0 °C to +70 °C -25°C to +125°C
MTBF	752000 h	
Humidity	5 – 95 % non-condensing	
Weight	65 g, no PC Card inserted	

Figure 2-1 : Technical Specification

3 Functional Description

The TPMC871 supports 16 bit PC Card 16 and 32 bit CardBus Cards. For 16 bit PC Card control the PCI1510 is fully register compatible with the Intel 82365L-DF PC Card interface controller through the ExCA register set. The ExCA registers can be accessed indirectly via PCI I/O access space or directly via PCI memory address space.

3.1 Address Mapping TPMC871 – PC Card 16 mode

The PCI1510 provides a window mechanism to link the PCI space to PC Card 16 address space. Memory and I/O windows are programmable by the host software in the ExCA registers of the PCI1510.

In PC Card 16 mode the TPMC871 Version 3.0 is fully compatible to the TPMC871 Version 1.0 and Version 2.0.

3.1.1 Memory Mapping

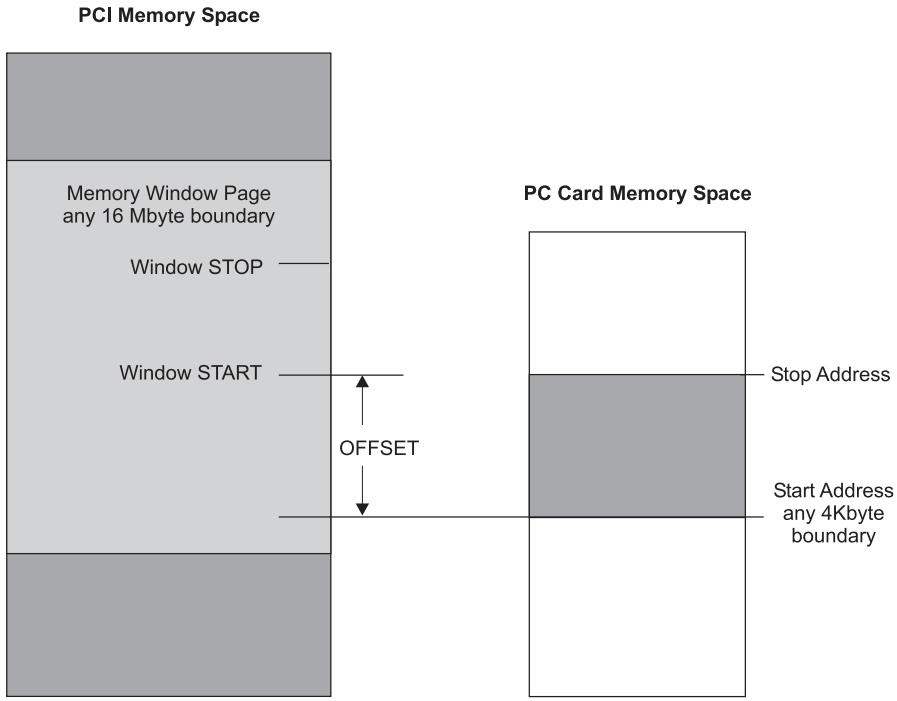

Figure 3-1 : PCI to PC Card memory mapping

To open a memory window, software must provide the PCI1510 with memory start address, memory stop address, PC Card memory offset and memory window page address.

PC Card memory is accessed only if the address window is enabled and if the memory address is located between start and stop address.

The Memory Window Page Register is only accessible via the PCI memory address space.

3.1.2 I/O Mapping

The 16 bit I/O card address space is accessed via 16 bit I/O addresses. The PC Card 16 I/O space is mapped to the lower 64kByte PCI I/O address space.

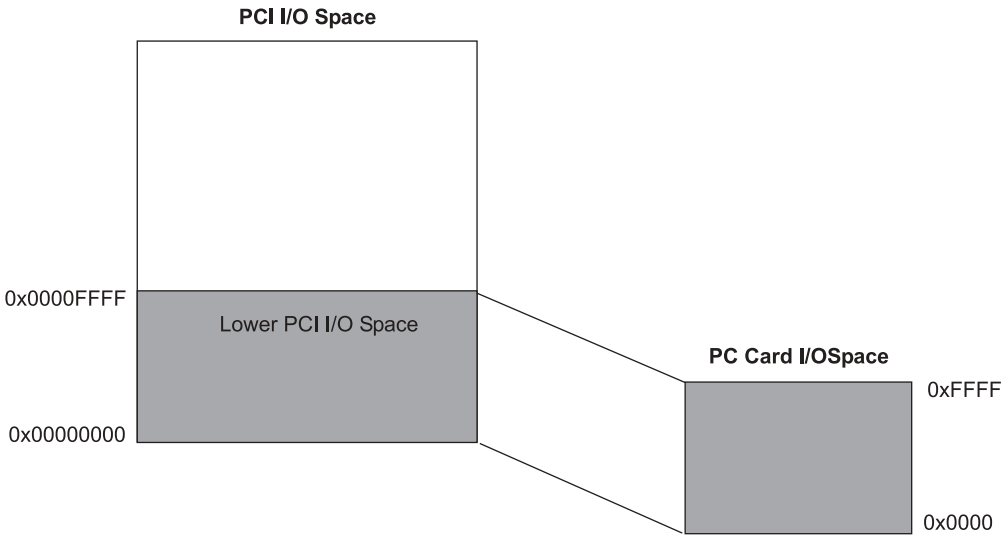

Figure 3-2 : PCI to PC Card I/O mapping

To open I/O window, software must provide the PCI1510 with I/O start address, I/O stop address, and I/O offset.

PC Card16 I/O is accessed only if the address window is enabled and if the I/O address is located between start and stop address.

For detailed information about window mapping procedure and status / control registers please refer to the PCI1510 data sheet which is part of the TPMC871-ED Engineering Documentation.

3.2 Address Mapping TPMC871 – CardBus mode

The PCI1510 provides a window mechanism to link the PCI space to 32 bit CardBus cards address space. Memory and I/O windows are programmable by the host software in the memory or I/O Base Register in the PCI1510 configuration space. The PCI1510 offers two memory and two I/O windows. The size of each window will be determined by host software via memory and I/O limit registers. The Base Address Register will be initialized with the start address and the limit registers will be initialized with the upper address of the memory or I/O window.

The CardBus card address space can be accessed via the CardBus base address registers, which are located in the PCI configuration space of the PCI1510.

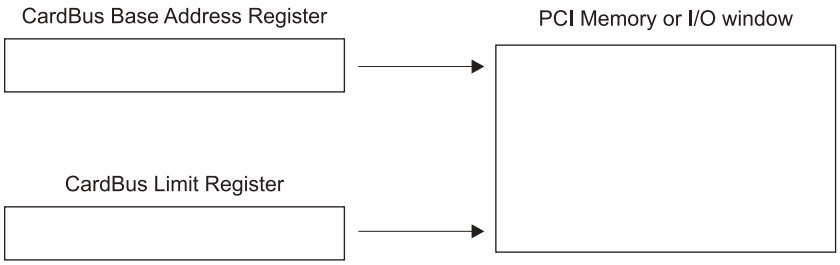

Figure 3-3 : CardBus window mechanism

The PCI1510 provides CardBus card status information via the CardBus Socket Register at configuration space offset 0x10. This address, which must be initialized by the device driver software, points to six 32 bit registers, which can be located anywhere in the PCI memory space at a 1Kbytes boundary at offset 0x00. The following socket registers are implemented in the PCI1510:

Register Name	Offset
Socket Event	0x00
Socket Mask	0x04
Socket Present State	0x08
Socket Force Event	0x0C
Socket Control	0x10
Reserved	0x14
Reserved	0x18
Reserved	0x1C
Socket Power Management	0x20

Figure 3-4 : Socket Registers implemented in PCI1510

These registers may notify the device driver software that a card has been inserted, removed, and what supply voltage is needed to power the CardBus card properly etc.

Further information regarding the status of the CardBus interface can be obtained from the secondary status register at offset 0x16 in the PCI configuration space of the PCI1510. This register is very similar to the PCI Bus Status Register and provides information about parity errors, aborted transactions, CardBus system errors etc.

For detailed register description, please refer to PCI1510 data sheet which is part of the TPMC871-ED Engineering Documentation.

3.3 PCI Interrupts

The multifunction pin 0 of the PC Card socket controller is used as the PCI interrupt INTA#. The PCI1510 provides a card status change interrupt which can notify the system of change in the PC Card battery voltage levels, PC Card insertion / removal detection, Ready/Busy# condition and functional status change. These various interrupt sources of the PC Card are individually programmable to INTA# via ExCA “Card Status Change Interrupt Configuration Register” at ExCA register offset 0x05.

4 PCI1510 PC Card Controller

4.1 PCI Configuration Registers

4.1.1 PCI Header of the TPMC871 Version 3.0

PCI CFG Register Address	31 24	23 16	15 8	7 0	PCI write able	Read after Reset (Hex-Value)
0x00	Device-ID		Vendor-ID		N	AC56104C
0x04	Status		Command		Y	02100000
0x08	Class Code			Revision ID	N	06070000
0x0C	BIST	Header Type	PCI Latency Timer	Cache line Size	Y[7:0]	00020000
0x10	CardBus Socket/ExCA Base Address				Y	00000000
0x14	Secondary Status		Reserved	Capability Pointer	N	020000A0
0x18	CardBus Latency Timer	Subordinate Bus Number	CardBus Bus Number	PCI Bus Number	Y	00000000
0x1C	CardBus Memory Base Register 0				Y	00000000
0x20	CardBus Memory Limit Register 0				Y	00000000
0x24	CardBus Memory Base Register 1				Y	00000000
0x28	CardBus Memory Limit Register 1				Y	00000000
0x2C	CardBus I/O Base Register 0				Y	00000000
0x30	CardBus I/O Limit Register 0				Y	00000000
0x34	CardBus I/O Base Register 1				Y	00000000
0x38	CardBus I/O Limit Register 1				Y	00000000
0x3C	Bridge Control Register		Interrupt Pin	Interrupt Line	Y	034001FF
0x40	Subsystem ID		Subsystem Vendor ID		Y	03671498
0x44	PC Card 16 I/F legacy mode base address				Y	00000001
0x48-0x7C	Reserved				N	00000000
0x80	System Control				Y	0804C020
0x84	Reserved				N	00000000
0x8C	Multifunction Routing				Y	00C11002
0x90	Diagnostic	Device Control	Card Control	Retry Status	Y	414400C0
0x94	Reserved				Y	00000000
0x98	Reserved				Y	00000000
0x9C	Reserved				N	00000000
0xA0	Power Management Capabilities		Next Item Pointer	Capability ID	N	7E220001
0xA4	PM data	PMCSR bridge support	Power Management status/control		Y	00C00000
0xA8	General Purpose Event Enable		General Purpose Event Status		Y	00000000
0xAC	General Purpose Output		General Purpose Input		Y	00000000
0xB0	Serial Bus Control /Status	Serial Bus Slave Address	Serial Bus Index	Serial Bus Data	Y	00000000
0xB4-0xFC	Reserved				N	00000000

Figure 4-1 : PCI Configuration Register

4.2 Configuration EEPROM

The TPMC871 is equipped with an on board I^2C EEPROM. After power-on or PCI reset, the following PCI Configuration Register of the PCI1510 PC Card controller will be initialized with hardware depended configuration data:

Register Name	Register Offset	EEPROM Offset	Value
Command Register	PCI 0x04	0x00	0x0000
Subsystem Vendor ID Register	PCI 0x40	0x02	0x1498
Subsystem ID Register	PCI 0x42	0x04	0x0367
PC Card 16-I/F LBAR	PCI 0x44	0x06	0x00000001
System Control Register	PCI 0x80	0x0A	0x0804C020
Multifunction Routing Register	PCI 0x8C	0x0E	0x00C11002
Retry Status Register	PCI 0x90	0x12	0xC0
Card Control Register	PCI 0x91	0x13	0x00
Device Control Register	PCI 0x92	0x14	0x44
Diagnostic Register	PCI 0x93	0x15	0x41
Power Management Capability	PCI 0xA2	0x16	0x7E
ExCA Identification and Revision	ExCA 0x00	0x17	0x84
Socket force Event	CB Socket + 0x0C	0x18	0x00

Address	Offset															
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC	0xD	0xE	0xF
0x00	0x01	0x00	0x98	0x14	0x67	0x03	0x01	0x00	0x00	0x00	0x20	0xC0	0x04	0x08	0x02	0x10
0x10	0xC1	0x00	0xC0	0x00	0x44	0x41	0x7E	0x84	0x00	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF

Figure 4-2 : Configuration EEPROM

The TPMC871 V3.0 Revision A shows the following differences in the PCI Configuration Registers:

Multifunction Routing Register (PCI 0x8C) = 0x00C10002

Device Control Register (PCI 0x92) = 0x40

4.3 ISA Interrupts

The TPMC871 provides a possibility to gain access to parallel or serialized ISA IRQ signals on board.

With the default EEPROM download configuration the PCI1510 is initialized to generate serial ISA IRQs on MFUNC3. For other IRQ configurations, the PCI1510 PC Card controller must be initialized through the controller's device driver. Interrupt signaling can be provided through the PCI1510 multifunction pins MFUNC3 and MFUNC6. MFUNC3 can be configured to function as serial or parallel ISA IRQ 2 to 15. MFUNC6 can be configured to function as parallel ISA IRQ 2 to 15. To enable the parallel ISA IRQs on these pins the following settings must be done by software:

Register	Offset	Required Value	ISA Routing
Multifunction routing	0x8C	Bits 27-24: 0x2 - 0xF	MFUNC6 is IRQ 2 -15
Multifunction routing	0x8C	Bits 15-12: 0x2 - 0xF	MFUNC3 is IRQ 2 -15
Device control	0x92	Bits 2–1: 0x01	Parallel ISA and PCI interrupts enabled
ExCA interrupt control	0x03	Bits 3-0: 0x3-0xF	IRQ 3-15 enabled

Figure 4-3 : ISA Interrupts

For further information please refer to the PCI1510 data sheet which is part of the TPMC871-ED Engineering Documentation.

Following figure shows where the ISA IRQ signal of MFUNC3 can be accessed on the flipside of the TPMC871:

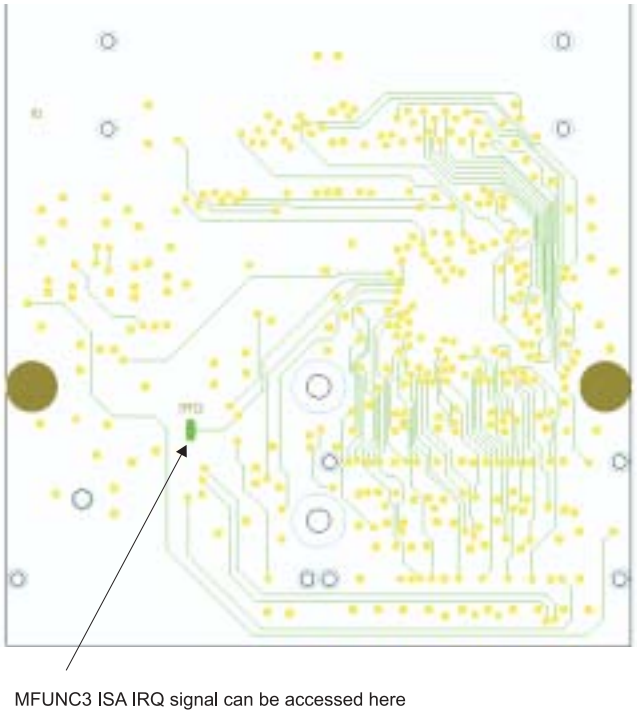

Figure 4-4 : ISA IRQ pad location

4.4 Initialization for CardBus mode

The TPMC871 V3.0 is initialized for PC Card16 mode per default. If 32 bit CardBus operation is wanted, a software device driver should perform the following initialization steps:

- The CardBus Latency Timer Register at offset 0x1B in the PCI Configuration space should be set to a value of 0x20.
- A Memory and/or the I/O Base Address Register must be written with a valid 32 bit window start address.
- A Memory and/or I/O Limit Register must be written with a valid 32 bit upper window address.