A GE Fanuc Company

VMIVME-7700

Ultra Low Voltage Intel® Celeron® VMEbus

- Intel®'s Ultra Low Voltage Celeron® 400 MHz/650 MHz processor
- Special features for embedded applications include:
  - Up to 1 GB bootable Flash on secondary IDE (optional)
  - Two 16-bit and two 32-bit programmable timers
  - 32 KB of nonvolatile SRAM
  - Software-selectable Watchdog timer with reset
  - Remote Ethernet booting
  - One PMC expansion site (IEEE-1386.1 PCI mezzanine card standard, 5 V)
  - VME64 modes supported: A32/A24/D32/D16/D08(EO)/MBLT64/BLT32
  - VMEbus interrupt handler, interrupter, and system controller
  - Includes real-time endian conversion hardware for little-endian and big-endian data interfacing (patent no. 6,032,212)
  - Enhanced bus error handling
  - Passive heat sink
  - Real-time clock and miniature speaker included
  - Dual front panel universal serial bus (USB) connections
- Standard features include:
  - Up to 512 MB PC100 SDRAM
  - 100 MHz system bus via Intel 815E chipset
  - Dual Ethernet controllers supporting 10BaseT and 100BaseTX interfaces
  - Ultra DMA/100 hard drive and floppy drive controllers (uses VMEbus P2 for connection to IDE/floppy)
  - Two high performance 16550-compatible serial ports
  - PS/2-style keyboard and mouse ports on front panel
  - VMEbus backplane interface
  - User programmable Watchdog timer
  - Passive processor heat sink

MICROPROCESSOR — The VMIVME-7700 is based on the Intel Ultra Low Voltage Celeron processor. The enhanced Celeron processor has 256 KB of on-die L2 cache. The µFCBGA package processors offer thermal characteristics that are well suited for embedded systems operating over a wide range of temperatures.

DRAM MEMORY — The VMIVME-7700 accepts one 144-pin SODIMM PC100 module for a maximum memory configuration of 512 MB.

BIOS — The VMIVME-7700 System BIOS and video BIOS are provided in reprogrammable memory.

VIDEO GRAPHIC CONTROLLER — High resolution graphics and multimedia-quality video are supported on the VMIVME-7700 by an internal 815E AGP graphics controller. A fully functional, integrated 2D/3D graphics accelerator provides pixel processing and rendering, with display resolutions of up to 1600 x 1200 supported. The video output is provided through the front panel.

CompactFlash — The VMIVME-7700 includes a CompactFlash socket on the assembly. The CompactFlash may be configured as the boot device through the BIOS boot device set up. The CompactFlash, as an ordering option, is available up to 1 GB of storage space.

IDE Interface — The VMIVME-7700 provides an IDE interface for hard disk drive support. The IDE interface allows support of several types of data transfers: Programmed I/O(PIO), 8237 style DMA, Ultra ATA/33, Ultra ATA/66 and Ultra ATA/100.

ETHERNET CONTROLLER — The VMIVME-7700 provides two front panel connections to either 10BaseT or 100BaseTX LAN using two Intel 82551ER Ethernet controllers. Standard RJ45 connectors are provided on the front panel with two network status indicators.

PHOTO NOT AVAILABLE

REMOTE ETHERNET BOOTING — The VMIVME-7700 utilizes an Expansion ROM BIOS which enables processor booting from a network server. The facility supports PXE and a variety of network boot protocols including BOOTP and DHCP (TCP/IP).

UNIVERSAL SERIAL BUS (USB) — The VMIVME-7700 provides front panel dual connection hub host controllers for the USB. Supported USB features include: isochronous data transfers, asynchronous messaging, self-identification and configuration of peripherals, and dynamic (hot) attachment.

SERIAL PORTS — The VMIVME-7700 provides two 16550-compatible serial ports. Each serial port has an independent 16-byte FIFO supporting baud rates up to 115 kbaud. Connection for both serial ports is provided by

Ordering Options

May 02, 2003 800-007700-000 A	A	B	C	–	D	E	F
VMIVME-7700 –				–			

A = Processor
- 0 = 400 MHz Ultra Low Voltage Celeron Processor
- 1 = 650 MHz Ultra Low Voltage Celeron Processor

B = SDRAM Memory
- 1 = 128 MB
- 2 = 512 MB

C = CompactFlash
- 0 = No CompactFlash
- 1 = 128 MB CompactFlash
- 2 = 256 MB CompactFlash
- 3 = 512 MB CompactFlash
- 4 = 1 GB CompactFlash

D/E = Reserved

Connector Adapter

VMIC Part Number 360-010050-01. The connector adapter is a 9-pin Micro-D to standard D serial adapter. The 360-010050-001 connector adapter is sold separately.

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com

two micro DB-9 connectors located on the front panel. The micro DB-9 connectors require two micro DB-9 to standard DB-9 adapters, VMIC P/N 360-010050-001.

PMC EXPANSION SITE — The VMIVME-7700 provides one IEEE 1386.1, 5 V PCI mezzanine card (PMC) expansion site. This expansion capability allows the addition of peripherals offered for PMC applications. The PMC site provides for standard I/O out the VMEbus front panel. An optional I/O connection to the VMEbus P2 connection can be provided.

KEYBOARD and MOUSE PORTS — The VMIVME-7700 supports a PS/2 keyboard and mouse through the front panel.

HARDWARE RESET — A hardware reset switch is accessible from the front panel.

PROGRAMMABLE TIMER — The VMIVME-7700 provides the user with two 16-bit timers and two 32-bit timers. These timers are mapped in PCI memory space, are completely software programmable and can generate PCI bus interrupts.

WATCHDOG TIMER — The VMIVME-7700 provides a software-programmable Watchdog timer. The Watchdog timer is enabled under software control. Once the timer is enabled, software must access the timer within the specified time period, or the output of the Watchdog timer will reset the unit.

NONVOLATILE SRAM — The VMIVME-7700 provides 32 KB of nonvolatile SRAM. The contents of the SRAM are preserved when +5 V power is interrupted or removed from the unit.

CMOS BATTERY — The VMIVME-7700 uses a holder that permits field replacement of the CMOS battery. A header and jumper allows the battery to be disconnected from the circuitry for long-term storage.

ANNUNCIATORS — Indicators for the board status, +5 V power good, are provided on the front panel. In addition, two indicators for the Ethernet adapter activity are located on each RJ45 network connector.

THERMAL MANAGEMENT — The VMIVME-7700 utilizes a passive heat sink that relies on forced air cooling within the equipment rack at the specified flow rate. Please refer to the environmental specifications for more information.

VMEbus INTERFACE — The VMIVME-7700 VMEbus interface is based on the Universe IID high performance PCI-to-VMEbus interface from Newbridge/Tundra.

SYSTEM CONTROLLER — The VMEbus system controller capabilities allow the board to operate as a slot 1 controller, or it can be disabled when another board is acting as the system controller. The system controller may be programmed to provide the following modes of arbitration:

Round Robin (RRS)

Single Level (SGL)

Priority (PRI)

The system controller provides a SYSCLK driver, IACK* daisy-chain driver, and a VMEbus access timeout timer. The system controller also provides an arbitration timeout if BBSY* is not seen within a specified period after a BGOUT* signal is issued. This period is programmable for 16 or 256 µs.

VMEbus REQUESTER — The microprocessor can request and gain control of the bus using any of the VMEbus request lines (BR3* to BR0*) under software control. The requester can be programmed to operate in any of the following modes:

Release-On-Request (ROR)

Release-When-Done (RWD)

VMEbus Capture and Hold (VCAP)

MAILBOXES — The VMEbus interface provides four 32-bit mailboxes, which are accessible from both the microprocessor and the VMEbus providing interprocessor communication. The mailboxes have the ability to interrupt the microprocessor when accessed by theVMEbus.

INTERRUPT HANDLER — The interrupt handler monitors, and can be programmed to respond to any or all VMEbus IRQ* lines. All normal-process VMEbus-related interrupts can be mapped to PCI INTA# or SERR# interrupts. These include:

Mailbox interrupts

VMEbus interrupts

VMEbus interrupter IACK cycle (acknowledgment of VMIVME-7700 VMEbus-issued interrupts)

All error processing VMEbus-related interrupts can be mapped to PCI INTA# or SERR#. Note: PCI SERR# initiates an SBC NMI. These include:

ACFAIL* interrupt

BERR* interrupt

SYSFAIL* interrupt

The interrupt handler has a corresponding STATUS/ID register for each IRQ* interrupt. Once the handler receives an IRQ*, it requests the VMEbus and, once granted, it performs an IACK cycle for that level. Once the IACK cycle is complete and the STATUS/ID is stored in the corresponding ID register, an appropriate interrupt status bit is set in an internal status register, and a PCI interrupt is generated. The PCI interrupt can be mapped to PCI INTA# or SERR#.

INTERRUPTER — Interrupts can be issued under software control on any or all of the seven VMEbus interrupt lines (IRQ7* to IRQ1*). A common ID register is associated with all interrupt lines. During the interrupt acknowledge cycle, the interrupter issues the ID to the interrupt handler. The interrupter can be programmed to generate a PCI INTA# or SERR# interrupt when a VMEbus interrupt handler acknowledges a software-generated VMEbus interrupt.

BYTE SWAPPING — The Intel 80x86 family of processors uses little-endian format. To accommodate VMEbus modules that transfer data in big-endian format, such as the 680x0 processor family, the VMIVME-7700 incorporates byte-swapping hardware. This provides independent byte swapping for both the master and slave interfaces. Both master and slave interface byte swapping are under software control. The VMIVME-7700 supports high throughput DMA transfers of bytes, words and longwords in both Master and Slave configurations. If endian conversion is not needed, we offer a special "bypass" mode that can be used to further enhance throughput. (Not available for byte transfers.)

MASTER INTERFACE — MA32: MBLT32: MBLT64 (A32:A24:A16:D32:D16:D8 (EO):BLT32)

The VMEbus master interface provides nine separate memory windows into VMEbus resources. Each window has separate configuration registers for mapping PCI bus transfers to the VMEbus (that is, PCI bus base address, window size, VMEbus base address, VMEbus access type, VMEbus address/data size, etc.). The maximum/minimum window sizes for the nine windows are as follows:

Window	Minimum Size	Maximum Size
0,4	4 KB	4 GB
1 to 3, 5 to 7	64 KB	4 GB
Special Cycle	64 MB	64 MB

SLAVE INTERFACE — Memory Access SAD032:SD32:SBLT32:SBLT64 (A32:A24:A16:D32:D16:D8 (EO): BLT32)

The VMEbus slave interface provides eight separate memory windows into PCI resources. Each window has separate configuration registers for mapping VMEbus transfers to the PCI bus (that is, VMEbus base address, window size, PCI base address, VMEbus access type, VMEbus address/data size, etc.). The maximum/minimum window sizes for the eight windows are as follows:

Window	Minimum Size	Maximum Size
0,4	4 KB	4 GB
1 to 3, 5 to 7	64 KB	4 GB

In addition, each window can be programmed to operate in coupled or decoupled mode. In decoupled mode, the window utilizes a write-posting FIFO and/or a read prefetching FIFO for increased system performance. In coupled mode, the FIFOs are bypassed and VMEbus transactions are directly coupled to the PCI bus (that is, transfers on VMEbus are not completed until they are completed on the PCI bus).

ENHANCED BUS ERROR HANDLING — Enhancements over the Universe chip's bus error handling features are provided. A latch and register are provided to allow the SBC to read the VMEbus address that caused the bus error in all modes. The Universe chip's support is limited to decoupled mode. Support for bus cycle timeout and assertion of bus error is provided. The board may be configured to assert bus error upon timeout regardless of its status as system controller. The Universe chip asserts bus error only if it is the system controller. In addition, this board may be configured to assert an interrupt upon bus cycle timeout.

BACK PANEL CONFIGURATION — The VMIVME-7700 provides support for external IDE disk drive and floppy drive through the VMEbus P2 backplane connector and the VMIACC-0562 backplane adapter.

OPERATING SYSTEM AND SOFTWARE SUPPORT — The VMIVME-7700 provides embedded features beyond PC/AT functionality. These features are supported by VMIC software products aimed at developers who are incorporating VMIC SBCs, I/O boards and workstations into systems. The VMIVME-7700 supports a variety of operating systems including Microsoft® Windows NT®, Windows® 2000, Windows XP, QNX, Linux® and VxWorks®.

SPECIFICATIONS

Single Slot 6U (4HP) Eurocard Form Factor:

Height 9.2 in. (233.4 mm)

Depth 6.3 in. (160 mm)

Thickness 0.8 in. (20.3 mm)

Power Requirements:

+5 VDC (±5 percent), <TBD> (typical), <TBD> mA maximum

+12 VDC (±5 percent), <TBD> (typical), <TBD> mA maximum

-12 VDC (±5 percent), <TBD> (typical), <TBD> mA maximum

NOTE: The currents at +12 and -12 VDC are specified with the serial connectors open.

Airflow:

Forced air cooling required: <TBD> LFM minimum

Temperature:

Operating: -20 to +70 ˚C
Storage : -40 to +80 ˚C

Altitude:

Operating: 0 – 10,000 ft (3,000m)
Storage: 0 – 40,000 ft (12,000m)

Humidity:

Operating, Relative Humidity 5 to 95% non-condensing
Storage, Relative Humidity 5 to 95% non-condensing

VMEbus Interface:

DTB Master: BLT32/BLT64, A32/D32, A24/D32, A16/D32
DTB Slave: BLT32/BLT64, A32/D32, A24/D32, A16/D32
Requester: Programmable, BR(3 to 0), ROR, RWD, BCAP
Interrupt Handler: IH(1 to 7) D8(O)
Interrupter: Programmable, IRQ7* to IRQ1*
Arbiter: SGL, PRI, RRS

BTO: Programmable (4 to 1,024 µs)
Compliance: ANSI/VITA 1-1994

PMC Expansion Site Connector: 5 V signaling, types 1 and 2 32-bit PCI bus, 33 MHz maximum

MTBF: <TBD>
Regulatory: CE Mark

TRADEMARKS

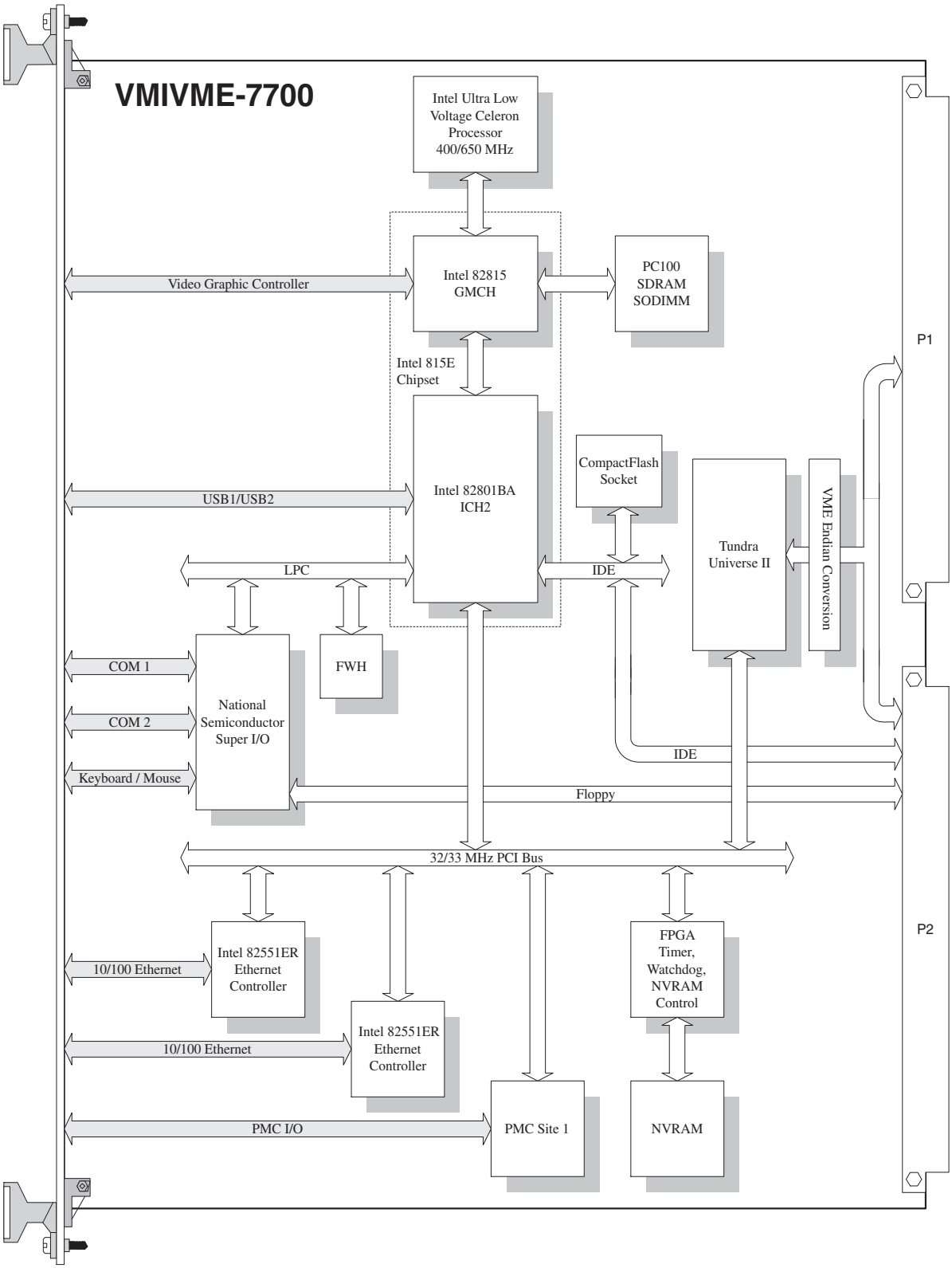

Figure 1. VMIVME-7700 Block Diagram