PPC/PowerCore-6750
Reference Guide

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Force Computers GmbH

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List of Tables and Figures

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Using This Manual

This section does not provide information on the product but on common features of the manual itself:

- Structure
- Special layout conventions
- Related documents.

Audience of the Reference Guide

The *Reference Guide* is intended for hard- and software developers installing and integrating the PPC/PowerCore-6750 into their systems.

Overview of the Reference Guide

The *Reference Guide* provides a comprehensive hardware and software guide to the board. It additionally includes the *PowerBoot Instruction Set*.

Note: **Please take a moment to examine the "Table of Contents" of the *Reference Guide* to see how this documentation is structured. This will be of value to you when looking for information in the future.**

Reference Guide

The *Reference Guide* includes:

- Brief overview of the product, the specifications, and the ordering information: see section 2 "Introduction" on page 5
- Installation instructions for powering up the board: see section 3 "Installation" on page 9. It includes the default configuration (switches and the like), initialization, and connector pinouts.

  The installation instructions also appear as the product's installation guide – a separate manual delivered together with each shipped product.
- Detailed hardware description: see section 4 "Hardware" on page 29
- Description of the board specific PowerBoot commands: see section 6 "PowerBoot for PPC/PowerCore-6750" on page 85

Data Sheets

The following data sheets are relevant for the PPC/PowerCore-6750. They contain information relevant for configuring and inegrating the board intosystems and can be found on the respective company's webpage:

- PCI-to-ISA Bridge – W83C553F (http://www.winbond.com)
- CIO Counter/Timer – CIO Z8536 (http://www.zilog.com)
- Real-Time Clock and NVRAM – RTC/NVRAM M48T58 (http://www.us.st.com)
- Serial I/O Port – TL16C550C (http://www.ti.com)
- Ethernet Controller – LAN 21143(http://www.developer,intel.com)
- Ethernet Interface Adapter – LXT970 and ICS 1890 (http://www.level1.com)
- VMEbus Interface PCI-to-VMEbridge – Universe II User's Guide (http://www.tundra.com)
- Grackle NPC106 (http://www.motorola.com)

PowerBoot Instruction Set

The *PowerBoot Instruction Set* describes only those PowerBoot commands which are independent of the CPU board. The board specific PowerBoot commands are described in the *Reference Guide* (see section 6 "PowerBoot for PPC/PowerCore-6750" on page 85).
The *PowerBoot Instruction Set* is packaged separately and always shipped together with the *Reference Guide*.

☞ **Insert the *PowerBoot Instruction Set* now: see section 5 "PowerBoot (= PowerBoot Instruction Set)".**

Table a **History of Manual Publication**

Edition	Date	Description
1.0	May 1998	First print
2.0	July 1998	SDRAM memory module description added. Technical Reference Manual corrected, revised, and extended.
2.1	December 1998	Excerpt from the data sheet's ordering information updated, power requirements and bus frequencies of the 300-MHz and 400-MHz boards included
3.0	March 1999	Edition increased

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Table a **History of Manual Publication**

Edition	Date	Description
4.0	September 1999	PowerBoot start-up banner changed, SETBOOT extended by Power ON test POT
5.0	February 2000	Changed manual type, changed Power-Boot User's Manual to Instruction Set, removed data sheet section, editorial changes
6.0	August 2000	Removed reference to Universe and Grackle Set of Data Sheets, editorial changes

Table b **Fonts, Notations and Conventions**

Notation	Description
`0000.0000`$_{16}$	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets. Note the dot marking the 4th (to its right) and 5th (to its left) digit.
`0000`$_{8}$	Same for octal numbers (digits are 0 through 7)
`0000`$_{2}$	Same for binary numbers (digits are 0 and 1)
`Program`	Typical character format used for names, values, and the like that should be used typing literally the same word. Also used for on-screen-output.
Variable	Typical character format for words that represent a part of a command, a programming statement, or the like and that will be replaced by an applicable value when actually applied.
#	A # symbol at the end of a PCI, ISA, or IDE signal name indicates that the signal is active when it is at low voltage. The absence of the # symbol indicates that the signal is active at high voltage.
*	A * symbol at the end of a VMEbus signal name indicates that the signal is active when it is at low voltage. The absence of the * symbol indicates that the signal is active at high voltage.

Register Conventions

Force Computers assumes that the software developer initializes the register bits which are not described with default settings.

Icons for Ease of Use: Safety Notes and Tips & Tricks

The following three types of safety notes appear in this manual. Be sure to always read and follow the safety notes of a section first – before acting as documented in the other parts of the section.

Danger

Dangerous situation: serious injuries to people or severe damage to objects.

Caution

Possibly dangerous situation: slight injuries to people or damage to objects possible.

Note: **No danger encountered. Pay attention to important information marked using this layout.**

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1 Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the PPC/PowerCore-6750. For your protection, follow all warnings and instructions found in the following text.

General

This *Reference Guide* provides the necessary information to install and handle the PPC/PowerCore-6750. As the product is complex and its usage manifold, we do not guarantee that the given information is complete. In case you need additional information, ask your Force Computers representative.

The PPC/PowerCore-6750 has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or qualified persons in electronics or electrical engineering are authorized to install, uninstall or maintain the PPC/PowerCore-6750. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Installation

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their life. Therefore:

- **Before installing the board, check:**
  - **section “Power Requirements” on page 10**
  - **and section “Thermal Requirements” on page 12**
- **Before touching integrated circuits, ensure that you are working in an electrostatic-free environment.**
- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or uninstalling the board, read section 3 “Installation” on page 9.**
- **Before installing or uninstalling an additional device or module, read the respective documentation.**

- **Ensure that the board is connected to the VMEbus via both the P1 and the P2 connectors and that the power is available on both VMEbus connectors.**

Operation

- **While operating the board ensure that the power and environmental requirements as given in table 4 “Typical Power Consumption of the CPU Board” on page 10 and table 7 “Environmental Requirements of PPC/PowerCore-6750” on page 12 are met.**
- **When operating the board in areas of strong electromagnetic radiation ensure that the board is bolted on the VME rack and shielded by closed housing.**

EMC

- **If boards are integrated into open systems, always cover empty slots.**
- **The front panel of the PPC/PowerCore-6750 provides 2 cutouts for the front panels of the PMC modules. If the board is shipped without the module installed, the front-panel cutouts are covered by blind panels to ensure proper EMC shielding. To ensure proper EMC shielding, always operate the PPC/PowerCore-6750 with the blind panel or with PMC modules installed.**

Expanding

- **Check the total power consumption of all components installed (see the technical specification of the respective components). For the total power consumption of the PPC/PowerCore-6750, see table 4 “Typical Power Consumption of the CPU Board” on page 10.**
- **Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).**
- **Only replace components or system parts with those recommended by Force Computers. In case you use components other than those recommended by Force Computers, you are fully responsible for the impact on EMI and the eventually changed functionality of the product.**

Environment

Always dispose used batteries and/or old boards according to your country’s legislation.

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Battery

If a Lithium battery on a board has to be exchanged, observe the following safety notes:

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Always use the same type of Lithium battery as is already installed.**

RJ-45 Connector

If an RJ-45 connector is available on the board, take into account that the RJ-45 connector type is used for telephone connectors and for twisted pair Ethernet (TPE) connectors. Note that mismatching these 2 connectors may destroy your telephone as well as your PPC/PowerCore-6750.
Therefore:

- **Make sure that TPE connectors near your working area are clearly marked as network connectors.**
- **Make sure that TPE bushing of the system is connected only to safety extra low voltage (SELV) circuits.**
- **Verify that the length of an electric cable connected to a TPE bushing does not exceed 1 kilometer outside the building.**
- **If in doubt, ask your system administrator.**

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2 Introduction

PPC/PowerCore-6750 is a high performance single-board computer providing a Universe VMEbus interface. It is based on

- Microprocessor PowerPC 750
- VMEbus

Memory

Per default PPC/PowerCore-6750 provides a shared memory implemented by one (lower) memory module of up to 128 MByte.
Depending on the memory module installed on the CPU board, the capacity of the shared memory may be increased by installing an upper memory module on top of the (lower) memory module.

The secondary (L2) cache has a size of up to 1 MByte. The boot flash has a maximum capacity of 2 MByte and the on-board user flash has a maximum capacity of 8 MByte.

Interfaces

PPC/PowerCore-6750 includes VMEbus interface, PCI bus interfaces, Ethernet interface, and 2 serial I/O ports to provide full single-board computer functionality. The serial I/O ports are available at the front panel via two 9-pin Micro D-Sub connectors.

CPU Speed

The PowerPC CPU runs with a minimum frequency of 233 MHz and provides cache snooping support in order to maintain cache coherency.

Real-Time Clock

A real-time clock with on-board battery backup is also available.

2.1 Specification

Table 1 Specification of the PPC/PowerCore-6750

Processor	PowerPC 750
Shared memory	up to 128-MByte (lower) memory module
PMC slots	2 slots for 32-bit PMC modules I/Os for both PMC modules on VME P2 connector
PCI-to-VME bridge	Universe II
Ethernet interface	Ethernet controller 10Base-T or 100Base-Tx on front panel
Two serial I/O ports	RS-232 compatible I/O on front panel
Counters/timers	Three 16-bit, programmable
Boot flash	Up to 2 MByte (512 KByte default) On-board programmable Hardware write protection
User flash	Up to 8 MByte On-board programmable Hardware write protection
RTC/SRAM/battery	Real-time clock and NVRAM
Additional features	Reset and abort key, status LEDs, serial PROM for board configuration, voltage sensors, watchdog timer
Firmware	PowerBoot
Power consumption	see section 3.1.1 “Requirements” on page 10
Environm. conditions	see subsection“Thermal Requirements” on page 12 and **table 7 “Environmental Requirements of PPC/PowerCore-6750” on page 12**.
Standards compliance	ANSI/VITA 1-1994 IEEE P1386.1/Draft 2.0

PPC/PowerCore-6750 is available in several memory and speed options. Consult your local sales representative to confirm availability of specific combinations.

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2.2 Product Nomenclature

Table 2 Nomenclature of the PPC/PowerCore-6750

PPC/PowerCore-6750/yyS-ccc-Llll-z	
750	PowerPC processor type 750
yyS	DRAM size in MByte, *S* means SDRAM
ccc	Processor clock frequency in MHz
Llll	L2 cache capacity in KByte
z	User flash capacity in MByte

2.3 Ordering Information

The following table is an excerpt from the PPC/PowerCore-6750 data sheet. Please ask your local Force Computers representative for the current PPC/PowerCore-6750 data sheet.

Table 3 Excerpt from the Data Sheet's Ordering Information

Product Name	Description
PPC/PowerCore-6750/…	
...16-233-L512-4-SSIO	PowerPC 750, 16-MByte EDO DRAM, 233-MHz nominal processor frequency, 512-KByte L2 cache, 4-MByte user flash, and SSIO
...128S-400-L1024-8	PowerPC 750, 128-MByte SDRAM, 400-MHz nominal processor frequency, 1-MByte L2 cache, and 8-MByte user flash
PPC/PowerCore-…	
...MEM/128U	user upgradable upper EDO DRAM memory module, 128 MByte
...SMEM/128U	user upgradable upper SDRAM memory module, 128 MByte
Accessories PPC/…	
…PPC/PowerCore-6750-SSIO/AccKit	PPC/IOBP-6750 including cables (see "I/O Panel" on page 25)
…PowerCore-6750 RG	*Reference Guide* for PPC/PowerCore-6750 including *PowerBoot Instruction Set*

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3 Installation

Note: **Before powering up or plugging the board in, read section 1 "Safety Notes" on page 1, check section 3.1 "Installation Prerequisites and Requirements" on page 10 , check the consistency of the current switch settings (see section 3.3 "Switch Settings" on page 15), and check the consistency of the current switch settings on the PPC/SSIO-6750 if a PPC/SSIO-6750 is installed (see the *PPC/SSIO-6750 Installation Guide*).**

Caution

To ensure proper functioning of the PPC/PowerCore-6750 board, remove the jumper for IACKIN-IACKOUT- and BGIN-BGOUT-bypass on the backplane. This is not necessary on active backplanes.

Note: **Before installing or uninstalling a PPC/PowerCore memory module, read the respective *Memory Module Installation Guide* packaged together with the memory module. Before installing or uninstalling a PMC module, read the PMC module's documentation.**

The CPU board is designed to be maintenance-free. However, note that a Lithium battery is installed on the board. The battery provides a data retention of 7 years summing up all periods of actual battery use. Therefore, Force Computers assumes that there usually is no need to exchange the Lithium battery except for example in the case of long-term spare part handling.

Caution

Observe the following safety notes:

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Exchange the battery before 7 years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, back up affected data before exchanging the battery.**
- **Always use the same type of Lithium battery as is already installed.**
- **When installing the new battery ensure that the marked dot on top of the battery covers the dot marked on the chip.**
- **Used bateries have to be disposed according to your country's legislation.**

3.1 Installation Prerequisites and Requirements

3.1.1 Requirements

The installation requires only

- Power supply
- Fan unit providing an airflow meeting the thermal requirements of the PPC/PowerCore-6750
- VMEbus backplane with P1 and P2 connectors

Power Requirements

PPC/PowerCore-6750 provides a limited current at the PMC supply pins. The maximum current depends on:

- CPU type and frequency
- Installed memory modules.

Typical power requirements of the CPU board are given in the following table:

Table 4 Typical Power Consumption of the CPU Board

CPU Board with Lower Memory Module but without PMC Module	+5V
PPC/PowerCore-6750/16-233-L512-4	3.1 A
PPC/PowerCore-6750/64-233-L512-4	3.1 A
PPC/PowerCore-6750/64S-300-L1024-8	4.1 A
PPC/PowerCore-6750/128S-300-L1024-8	4.2 A
PPC/PowerCore-6750/64S-400-L1024-8	4.2 A
PPC/PowerCore-6750/128S-400-L1024-8	4.4 A
PPC/PowerCore-6750/64S-400-L1024-8-SSIO	4.4 A

Memory Modules

Per default the shared memory of the CPU board is provided by one (lower) memory module directly located on the CPU board. The following two types of memory modules are available:

- EDO DRAM memory module
- SDRAM memory module

If your CPU board is equipped with one of the following lower memory modules, you may increase the capacity of the shared memory by install-

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ing an additional appropriate (upper) memory module on top of the lower one:

- 64-MByte EDO DRAM memory module
- 64- or 128-MByte SDRAM memory module

All other memory modules per default installed on the board, for example the 16-MByte EDO DRAM memory module, cannot be upgraded.

Caution

When installing or uninstalling a memory module, observe the following safety notes:

- **PPC/PowerCore-6750 may be equipped only with memory modules qualified by Force Computers. Otherwise the board or connected components may be damaged.**
- **On PPC/PowerCore-6750 revision 1.0 only EDO DRAM memory modules may be installed, i.e. it is not allowed to install SDRAM memory modules on boards of revision 1.0.**
- **Do not place an EDO DRAM memory module on top of an SDRAM memory module or vice versa.**

Out of the comprehensive list of possible configurations the memory configurations shown in the following table have been qualified.

Table 5 Qualified Memory Module Configurations

	PPC/PowerCore-…	
	MEM/128U	**SMEM/128U**
PPC/PowerCore-6750/64-…	x	–
PPC/PowerCore-6750/64S-…	–	x
PPC/PowerCore-6750/128S-…	–	x

The upgrading instructions are shipped together with the memory modules: see the respective *Memory Module Installation Guide.*

When installing an upper memory module on the lower memory module installed per default on the CPU board, you have to consider the power consumption. In this case add

- Power consumption of the CPU board including lower memory module (see table 4 “Typical Power Consumption of the CPU Board” on page 10)
- Max. power consumption drawn by the upper memory module (see table 6 “Max. Power Consumption of the Upper Memory Modules”).

Table 6 Max. Power Consumption of the Upper Memory Modules

PPC/PowerCore-…	3.3 V
MEM/128U	0.1 A
SMEM/128U	0.2 A

PMC

The total maximum permissible power consumption of all PMC modules installed on a CPU board with a lower memory module is 15 W.
If additionally an upper memory module is installed, the max. permissible power consumption values of the PMC modules are reduced by the max. power consumption value of the upper memory module (see table 6 “Max. Power Consumption of the Upper Memory Modules” on page 12).

Thermal Requirements

The operating temperature is 0×C to +55×C (humidity 5% to 95% noncondensing at +40×C), when operating the PPC/PowerCore-6750 in systems providing a minimum forced airflow of 300 LFM (linear feet per minute). The airflow is required at the heat sink of the CPU and at the top side of the CPU board. The typical operating temperature of the system is 0°C to +40°C. The following table summarizes the environmental requirements of the PPC/PowerCore-6750.

Table 7 Environmental Requirements of PPC/PowerCore-6750

	Operating	Non-Operating
Temperature	0°C to +55°C	–40°C to +85°C
Forced Air Flow	300 LFM (linear feet per minute)	–
Temp. Change	+/– 0.5°C/min	+/– 1°C/min
Rel. Humidity	5% to 95% noncondensing at +40°C	5% to 95% noncondensing at +40°C
Altitude	–300 m to +3.000 m	–300 m to +13.000 m

Backplane Configuration

The CPU board includes an IACK daisy-chain driver. If the CPU board is plugged in slot 1 and configured accordingly by SW7-1 (see table 8 “Default Switch Settings” on page 16), the board acts as IACK daisy-chain driver. Plugged in any other slot the board closes the IACKIN-IACKOUT path. Therefore:

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If not on an active backplane,

- Remove the jumper on the backplane connecting BG3IN* and BG3OUT* for the PPC/PowerCore-6750 slots which actually are connected to the backplane.
- Assemble the jumpers for BG3IN* and BG3OUT* on lower and higher slots on the backplane where no board is plugged.

Slot-1 Function

If more than one system controller is active in the VMEbus system, the board or other VMEbus participants can be damaged. Therefore, ensure that only one CPU board is configured to be system controller in the VMEbus system.

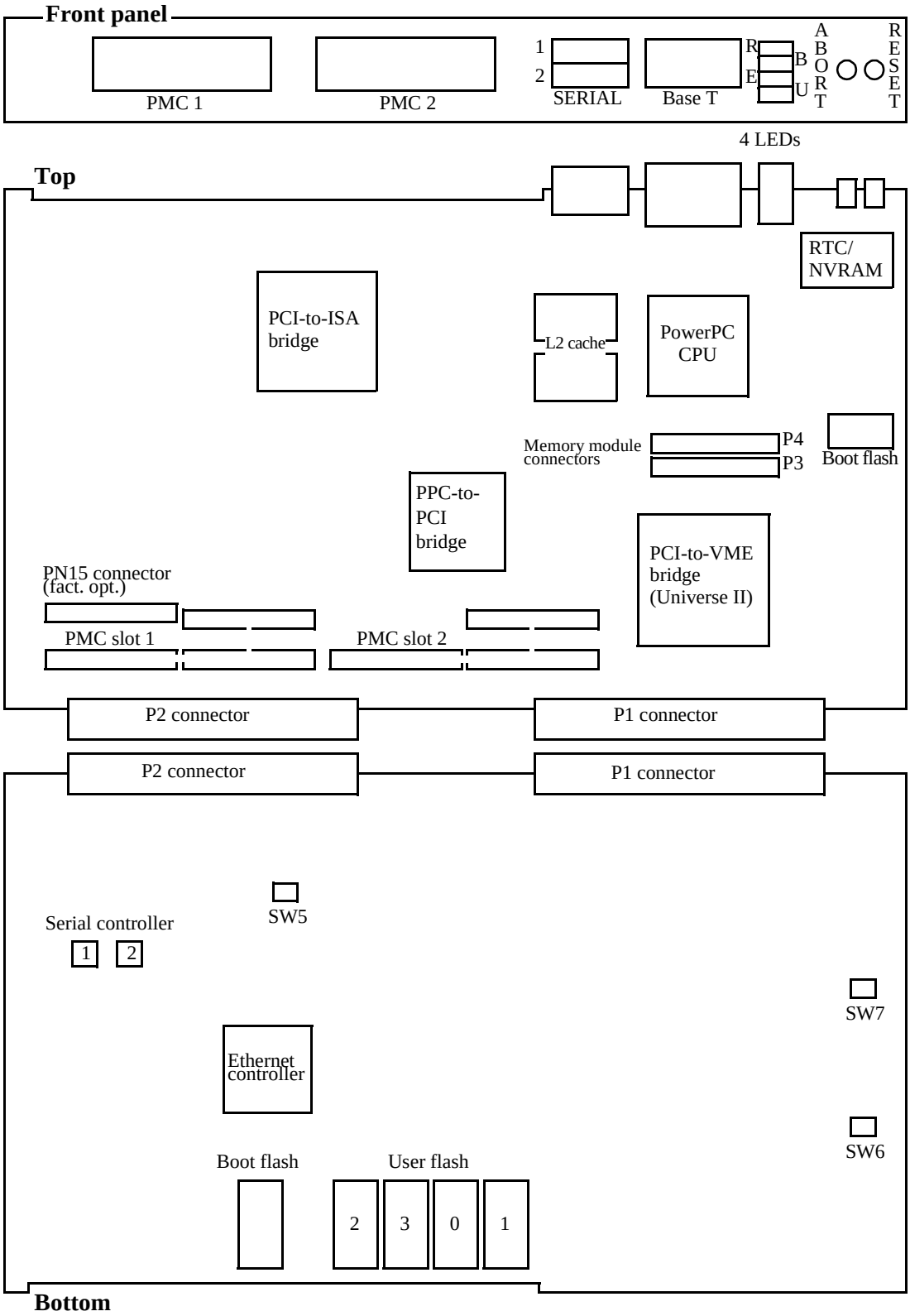
3.1.2 Terminal Connection

For the initial power-up, a terminal can be connected to the 9-pin MicroD-Sub connector of the serial port 1, which is located at the front panel (see section 3.6 “Serial I/O Ports” on page 20).

3.1.3 Location Overview

The figure 1 “Location Diagram of the PPC/PowerCore-6750 (schematic)” on page 14 highlights the position of the important PPC/PowerCore-6750 components. Depending on the board type it might be that your board does not include all components named in the location diagram.

Figure 1 Location Diagram of the PPC/PowerCore-6750 (schematic)



3.1.4 Upgrading PPC/PowerCore-6750

Memory Module

Depending on the (lower) memory module, which is per default installed, the memory capacity of the PPC/PowerCore-6750 may be increased by installing an upper memory module on the (lower) memory module.
For detailed information on the memory modules, see

- section 3.1.1 “Requirements” on page 10
- The respective *Memory Module Installation Guide*

PMC Module

PPC/PowerCore-6750 provides 2 PMC slots. The PMC slots can be used to install PMC modules based on the PCI bus architecture.
For detailed information on the PMC slots, see

- section 3.1.1 “Requirements” on page 10
- section 3.7 “PMC Slots” on page 21

3.2 Automatic Power Up – Voltage Sensor and Watchdog Timer

Voltage Sensors

If the voltage levels drop below the voltage values given in the VMEbus specification, the voltage sensors generate automatically a reset of the CPU board and proceed with a normal booting procedure.

Watchdog Timer

Per factory default the watchdog timer is disabled. If the watchdog timer is enabled, it generates a non-maskable interrupt (NMI) followed by a reset when it is not retriggered by the software. The watchdog timer can be enabled by SW5-1 (see “SW5-1” on page 16).

3.3 Switch Settings

The following table lists the functions and the default settings of all switches shown in figure 1 “Location Diagram of the PPC/PowerCore-6750 (schematic)” on page 14. The switches are located on the bottom side of the CPU board. For switching it is not required to remove any modules.

Caution

- **Before powering up the board check the current switch settings for consistency.**
- **SW7-1, SW7-2, and SW7-3 will only be read on a power up.**
- **Do not switch during operation.**

Table 8 Default Switch Settings

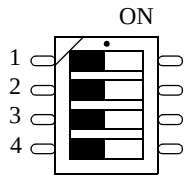
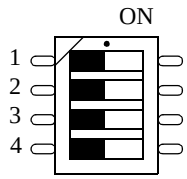
Name and Default Setting		Description
	SW5-1 OFF	Watchdog timer OFF = Timer disabled ON = Timer enabled
	SW5-2 OFF	Watchdog time (±±±±8ms) OFF = NMI: 39 ms, RESET: 134 ms ON = NMI: 363 ms, RESET: 1.66 s
	SW5-3 OFF	VMEbus SYSRESET input OFF = SYSRESET generates power up reset ON = SYSRESET does not generate power up reset
	SW5-4 OFF	Reserved
	SW6-1 OFF	RESET key OFF = RESET key enabled ON = RESET key disabled
	SW6-2 OFF	ABORT key OFF = ABORT key enabled ON = ABORT key disabled
	SW6-3 OFF	User flash write protection OFF = writing enabled ON = write-protected
	SW6-4 OFF	Boot flash write protection OFF = write-protected ON = writing enabled

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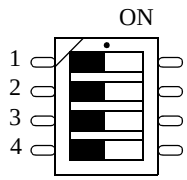
Table 8 Default Switch Settings (cont.)

Name and Default Setting		Description
	SW7-1 OFF	VMEbus slot 1 auto-detection OFF = enabled ON = disabled (also called manual mode)
	SW7-2 OFF	System controller (only available if SW7-1 = ON) OFF = disabled ON = enabled
	SW7-3 OFF	Power up detection level OFF = conforms to ANSI/VITA 1-1994 ON = below ANSI/VITA 1-1994 (This has the advantage that sudden voltage sags do not generate a reset.)
	SW7-4 OFF	VMEbus SYSRESET output OFF = enabled ON = disabled

3.4 Front Panel

The features of the front panel are described in the following sections. For a location diagram see figure 1 “Location Diagram of the PPC/PowerCore-6750 (schematic)” on page 14.

Table 9 Front-Panel Features

Device	Description
RESET	Mechanical reset key: When enabled and toggled it instantaneously affects the CPU board by generating a reset. Depending on SW7-4 the reset generates a VMEbus SYSRESET (see “SW7-4” on page 17). A reset of all on-board I/O devices and the CPU is performed when the reset key is pushed to the active position. RESET is held active until the key is back in the inactive position, however at least 200 ms are guaranteed by a local timer. Power fail (below approximately 4.7 V) and power up – both lasting at minimum 200 ms to 300 ms – also force a reset to start the CPU board. For information on enabling the key, see “SW6-1” on page 16.
ABORT	Mechanical abort key: When enabled and toggled it instantaneously affects the CPU board by generating an interrupt request (NMI) via the PCI-to-ISA bridge. This allows to implement an abort of the current program, to trigger a self-test or to start a maintenance program. For information on enabling the key, see “SW6-2” on page 16.
LED R	RUN/RESET LED indicating the board status: Green: normal operation Red: reset is active
LED B	VMEbus master and SYSFAIL LED: Green: when the CPU board accesses the VMEbus as VMEbus master Red: when the CPU board drives SYSFAIL on the VMEbus Off: otherwise
LED E	Ethernet LED: Green: transmit data Red: receive data Off: no traffic
LED U	User LED: Software programmable by the CIO counter/timer and parallel I/O unit. Bits 0 and 1 of port C are used. Possible status: green, red, or off.
100Base-Tx /10Base-T ETHERNET	An 8-pin RJ45 connector for 100Base-Tx or 10Base-T Ethernet interface.
SERIAL PORTS	Two 9-pin MicroD-Sub connectors for serial interface 1 and 2 (see section 3.6 “Serial I/O Ports” on page 20).

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3.5 PPC/PowerCore-6750 Parameters and Timers – CIO

Device: CIO	
Frequency	4.125 MHz
Accessible from	PowerPC processor
Access base address	ISA: 0000.0300_{16} PCI: 0000.0300_{16} CPU: $FE00.0300_{16}$
Port width	8 bit
Interrupt request	Priority level 3 (software reprogrammable, IRQ8#)

Configurable Parameters

Via the CIO device several parameters can be configured or read, respectively: programming voltage V_{PP}, user flash device select, user flash page select, boot flash page select (if boot flash has a capacity of 1 MByte or more), VMEbus SYSRESET out, watchdog trigger, user LED control, ID-ROM (serial EEPROM), PCI busmode signals, and the three 16-bit timers.

Timers

Three 16-bit timers with a resolution of approximately 500 ns are available.

3.6 Serial I/O Ports

PPC/PowerCore-6750 provides 2 serial I/O ports:

- Serial I/O port 1
- Serial I/O port 2

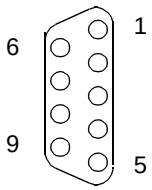
	Serial I/O Port 1	Serial I/O Port 2
Frequency	1.8432 MHz	
Accessible from	PowerPC processor	
Access Base Address	ISA: $0000.03F8_{16}$ PCI: $0000.03F8_{16}$ CPU: $FE00.03F8_{16}$	ISA: $0000.02F8_{16}$ PCI: $0000.02F8_{16}$ CPU: $FE00.02F8_{16}$
Port Width	8 bit	
Interrupt Request	Priority level 12 (software reprogrammable, IRQ4)	Priority level 11 (software reprogrammable, IRQ3)

Connector Availability

The RS-232 serial I/O ports 1 and 2 are each available via a 9-pin MicroD-Sub connector at the front panel.

Table 10 Pinout of the Front-Panel Serial I/O Port 1 and 2

9-pin MicroD-Sub



Pin	Signal
1	DCD (Data Carrier Detect, input)
2	RXD (Receive Data, input)
3	TXD (Transmit Data, output)
4	DTR (Data Terminal Ready, output)
5	GND (Ground)
6	DSR (Data Set Ready, input)
7	RTS (Request to Send, output)
8	CTS (Clear to Send, input)
9	GND (Ground)

Port Setup

- RS-232 asynchronous communication
- 9600 baud, 8 data bits, 1 stop bit, no parity
- No handshake protocol used per default

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3.7 PMC Slots

PPC/PowerCore-6750 provides 2 PMC slots for installing PMC modules compliant with IEEE P1386 ("Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC"). The PCI bus, a high speed local bus, connects different high speed I/O cards with PPC/PowerCore-6750. Both PMC slots support 32-bit data bus width with a frequency of 33 MHz.

Power of the PMC Modules

For information on the power of the PMC modules, see section 3.1 “Installation Prerequisites and Requirements” on page 10.

3.7.1 PMC Voltage Keys

The PCI bus uses a 5-V voltage to signal bus levels. The voltage keys prevent 3.3V PMC cards from being plugged into the PMC slots.

3.7.2 Connector Configuration

The 32-bit PCI bus requires 2 PMC connectors. The 3rd PMC connector connects additional user I/O signals of PMC slot 1 and PMC slot 2 with the VMEbus P2 connector rows A, C, D, and Z.

PMC slot 1 Connectors

- For the PCI bus: PN11 and PN12
- For 64 user I/O signals: PN14

PMC slot 2 Connectors

- For the PCI bus: PN21 and PN22
- For 64 user I/O signals: PN24

Caution

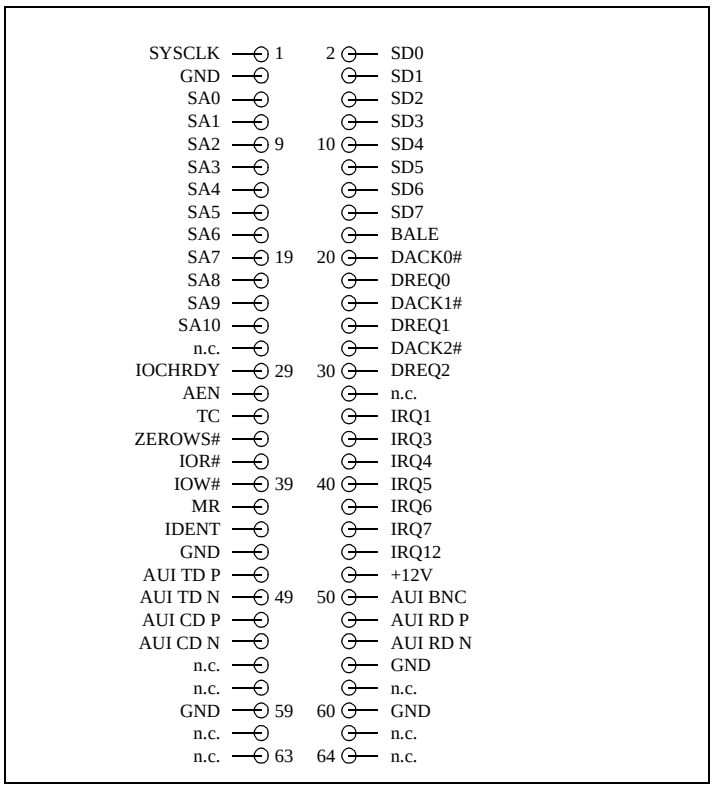
PMC slot 1 has 64 user I/O signals, which are all routed to the 64 user I/O pins of the VMEbus P2 connector row A and C (see figure 3 “P2 Connector Pinout, Row A and C” on page 24).
PMC slot 2 has also 64 user I/O signals, but only 46 of them are routed to the 46 available user I/O pins of the VMEbus P2 connector row Z and D (see figure 4 “P2 Connector Pinout, Row Z and D” on page 25). The user I/O signals 47…64 are not available.

3.7.3 ISA Connector

The connector PN15 is a factory option and makes a set of ISA bus signals available including differential AUI signals.

The following figure shows the signals available on the ISA connector.

Figure 2 **PN15 Connector Pinout**



3.8 Ethernet Interface

Device: Ethernet controller	
Frequency	PCI bus frequency: 33 MHz
Accessible from	PowerPC processor
Access base address	PCI: 0080.0000_{16} CPU: $FE85.0000_{16}$
Port width	32 bit
Interrupt request	Priority level 5 (INTA#, IRQ10)

The Ethernet 100Base-Tx or 10Base-T interface is available at the front panel via an 8-pin RJ45 connector.

If a PPC/SSIO-6750 is installed, the Ethernet interface is available at 2 Ethernet ports. The first port is at the front panel of the PPC/PowerCore-6750 base board (default). The second port is at the VMEbus connector P2.

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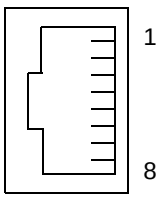
Caution

Use the Ethernet interface either at the front panel of the CPU board or at the VMEbus connector P2, not both. Check the configuration of the I/O panel.

To enable the Ethernet interface at the VMEbus connector P2, the software has to be set accordingly.

The PCI bus interface is 32-bit wide and able to transfer data via the on-chip DMA with programmable PCI burst size.
The following table shows the pinout of the Ethernet connector installed per default.

Table 11 8-Pin RJ45 Connector



Pin	Signal
1	TXP
2	TXM
3	RXP
4	n.c.
5	n.c.
6	RXM
7	n.c.
8	n.c.

3.9 VMEbus Interface – Universe II

Device: Universe II	
Frequency	PCI bus frequency: 33 MHz
Accessible from	PowerPC processor and VMEbus masters
Access base address	PCI: 0081.0000_{16} CPU: $FE81.0000_{16}$
PCI bus width	32 bit
Interrupt request	Priority level 6 (INTB#, IRQ11)

Universe II is a PCI-to-VME interface, which is able to transfer data via the programmable DMA controller with linked list support. Furthermore,

it provides full VMEbus system controller functionality and a PCI bus interface of up to 33 MHz.

3.10 VMEbus P2 Connector Pinout

The following 2 figures show the I/O signals available at the VMEbus P2 connector.
The figure 3 “P2 Connector Pinout, Row A and C” shows the PMC 1 I/O signals and figure 4 “P2 Connector Pinout, Row Z and D” shows the PMC 2 I/O signals (see section 3.7.2 “Connector Configuration” on page 21).

Figure 3 P2 Connector Pinout, Row A and C

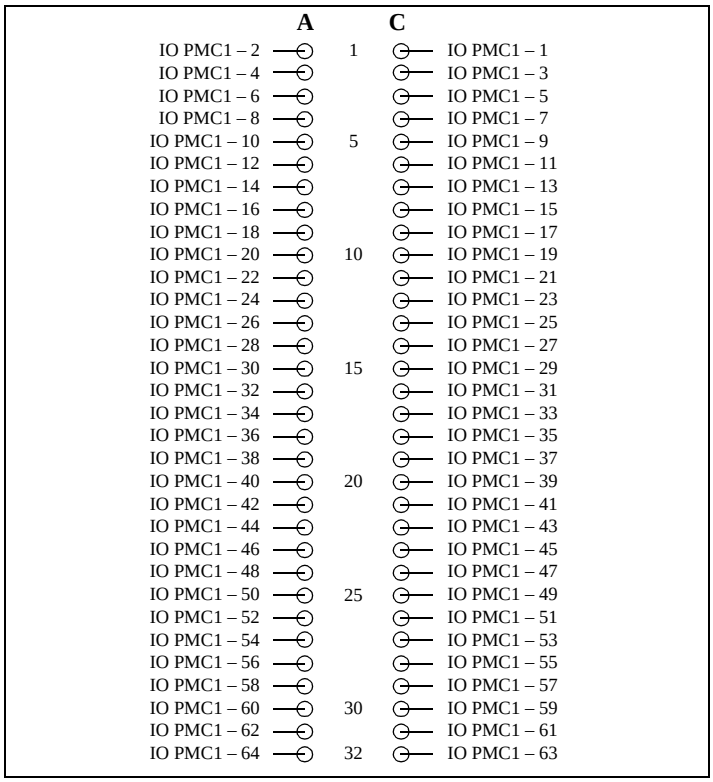


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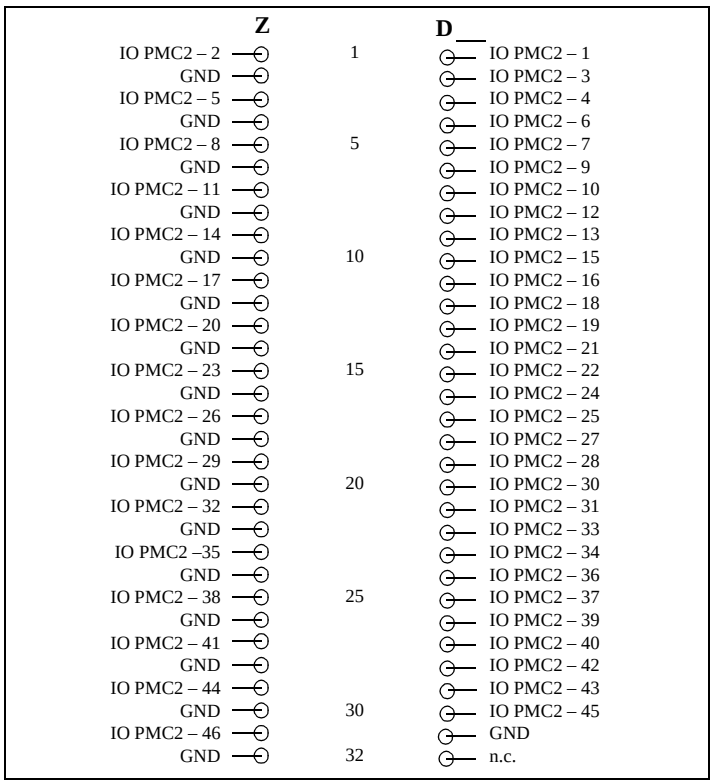
Figure 4 **P2 Connector Pinout, Row Z and D**



I/O Panel

As a separate price list item a 5-row I/O panel is available for the PPC/PowerCore-6750-SSIO, the PPC/IOBP-6750. The corresponding PPC/PowerCore-6750-SSIO Accessory Kit contains the following cables in addition to the I/O panel itself:

- Four serial flat-ribbon cables for the I/O panel
- One flat-ribbon SCSI cable for the I/O panel
- One Ethernet cable including panel

The PPC/PowerCore-6750-SSIO and the I/O panel support the following additional interfaces:

- Four serial interfaces
- One SCSI interface
- One AUI Ethernet interface

Caution

The PPC/IOBP-6750 is especially designed for the PPC/PowerCore-6750-SSIO. Do not use any other I/O panels on the PPC/PowerCore-6750-SSIO. Use the Ethernet interface either at the front panel of the CPU board or at the VMEbus connector P2, not both. Check the configuration of your I/O panel.

3.11 Testing the CPU Board Using PowerBoot

PowerBoot is firmware providing some basic test and debug commands. It is stored in the on-board boot PROM.

Booting up PowerBoot

PowerBoot automatically starts during power up or reset. After the successful pass of the self-initialization routine, the following message or a similar one will appear on the screen:

```
Init serial 1 at address: 0xFE0003F8
Init serial 2 at address: 0xFE0002F8
Init CIO at address: 0xFE000300
Init Ethernet Controller at address: 0xFE850000
Init UNIVERSE VMEbus device at address: 0xFE810000
PowerCore is -NOT- VMEbus System Controller (SYSCON=0)
Testing NVRAM.....................done
Testing RAM ......................done
Testing Boot FLASH....CSUM 0x20A7..done
Testing PCI Bus ..................done
Testing ISA ......................done
Testing Ethernet Controller........done
Found CPU740/750, PVR=00088201,
CPU clock: 233MHz, Bus clock: 66MHz
DRAM EDO mode enabled, DRAM ECC mode enabled
Onboard DRAM      : none
Init DRAM Module 1:  16MB, 0x00000000..0x00FFFFFF
Init DRAM Module 2:  none
Init DTLB/ITLB for block translation, enable MMU
Init L1-Icache
Init L1-Dcache
Init L2-Cache, found 1024 kByte cache, 146MHz
Init exception vectors starting at address: 0x00000100
Read NVRAM...identify board

<<PowerBoot V2.03 for PowerCore CPU-6750 VME>>

PowerBoot>
```

System Controller

If the board is configured as system controller, the user LED at the front panel turns green.

Starting a Test after Booting

To test the CPU board for correct operation enter `probepci`. `Probepci` does not provide a full-featured power-on self-test. Howev-

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er, it tests some I/O devices and scans the PCI bus for participants. Depending on the board configuration, the following message will appear:

```
 PowerBoot> probepci
Probing PCIbus at 0x80000000
Device ID = 0x0002; Vendor ID = 0x1057;
Status    = 0x0080; Command   = 0x0146;
Base Class= 0x06;   Sub Class = 0x00;   Prg. Inter= 0x00;   Rev. ID   = 0x40;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x00;   Cache Line= 0x08;
base addr0= 0x00000000, base addr1= 0x00000000;
Max Lat   = 0x00;   Min Gnt   = 0x00;   IRQ Pin   = 0x00;   IRQ Line  = 0x00;
Found PCI device: Motorola MPC106 PowerPC PCI bridge

Probing PCIbus at 0x8000C000
Device ID = 0x0000; Vendor ID = 0x10E3;
Status    = 0x0200; Command   = 0x0007;
Base Class= 0x06;   Sub Class = 0x80;   Prg. Inter= 0x00;   Rev. ID   = 0x01;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x20;   Cache Line= 0x00;
base addr0= 0x00810001, base addr1= 0xFFFFF000;
Max Lat   = 0x00;   Min Gnt   = 0x03;   IRQ Pin   = 0x01;   IRQ Line  = 0x00;
Found PCI device: Tundra UNIVERSE VMEbus interface

Probing PCIbus at 0x8000D000
Device ID = 0x0565; Vendor ID = 0x10AD;
Status    = 0x0200; Command   = 0x0007;
Base Class= 0x06;   Sub Class = 0x01;   Prg. Inter= 0x00;   Rev. ID   = 0x10;
BIST      = 0x00;   Header Typ= 0x80;   Latency Ti= 0x00;   Cache Line= 0x00;
base addr0= 0x00000000, base addr1= 0x00000000;
Max Lat   = 0x00;   Min Gnt   = 0x00;   IRQ Pin   = 0x00;   IRQ Line  = 0x00;
Found PCI device: Winbond W83C553F Sys. I/O Con., function 0

Probing PCIbus at 0x8000D100
Device ID = 0x0105; Vendor ID = 0x10AD;
Status    = 0x0280; Command   = 0x0000;
Base Class= 0x01;   Sub Class = 0x01;   Prg. Inter= 0x8F;   Rev. ID   = 0x05;
BIST      = 0x00;   Header Typ= 0x80;   Latency Ti= 0x00;   Cache Line= 0x08;
base addr0= 0x000001F1, base addr1= 0x000003F5;
Max Lat   = 0x28;   Min Gnt   = 0x02;   IRQ Pin   = 0x01;   IRQ Line  = 0x0E;
Found PCI device: Winbond W83C553F IDE, function 1

Probing PCIbus at 0x8000D800
Device ID = 0x0019; Vendor ID = 0x1011;
Status    = 0x0280; Command   = 0x0005;
Base Class= 0x02;   Sub Class = 0x00;   Prg. Inter= 0x00;   Rev. ID   = 0x30;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x20;   Cache Line= 0x00;
base addr0= 0x00850001, base addr1= 0xFFFFFF80;
Max Lat   = 0x28;   Min Gnt   = 0x14;   IRQ Pin   = 0x01;   IRQ Line  = 0x97;
Found PCI device: DEC 21143 PCI/Cardbus Ethernet LAN

Probing PCIbus at 0x8000F800
PowerBoot>
```

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4 Hardware

PPC/PowerCore-6750 is a high-performance single-slot PowerPC based platform providing a 64-bit VMEbus interface. The VMEbus interface device is directly connected to the PCI bus. The CPU board is based on:

- PowerPC CPU (see section 4.3 “PowerPC CPU” on page 40)
- VMEbus (see section 4.10 “PCI-to-VME Bridge – Universe II” on page 58)

Features

PPC/PowerCore-6750 provides:

- Watchdog timer (see section 4.5 “Watchdog Timer” on page 42)
- Shared memory implemented via a memory module (see section 4.6 “Shared Memory” on page 43)
- Boot flash (see section 4.7 “Boot Flash” on page 49)
- User flash (see section 4.8 “User Flash” on page 53)
- VMEbus interface (see section 4.10 “PCI-to-VME Bridge – Universe II” on page 58)
- Ethernet interface available via the front panel (see section 4.11 “Ethernet Interface” on page 67)
- On-board real-time clock with on-board battery backup (see section 4.13 “Real-Time Clock / Non-Volatile RAM” on page 71)
- Two RS-232 compatible serial I/O ports (see section 4.15 “Serial I/O Ports – SCCs” on page 76)
- Two PMC slots with user I/Os available at the 5-row VMEbus P2 connector (see section 4.16 “PMC Slots” on page 77)

DMA Controllers

The following devices are collectively referred to as DMA controllers of PPC/PowerCore-6750 because they themselves provide an on-chip DMA controller:

- Universe II
- PCI-to-ISA bridge
- Ethernet controller

Front-Panel Interfaces

The front panel of PPC/PowerCore-6750 provides:

- Ethernet interface for 10Base-T or 100Base-Tx (see section 4.11 “Ethernet Interface” on page 67)
- Two serial ports (see section 4.15 “Serial I/O Ports – SCCs” on page 76). These ports serve as console port, for download and for data communication

VMEbus P2 Connector

On the five-row VMEbus P2 connector the I/O signals of the PMC slots are available.

Factory Options

The following factory options are available:

- Type and capacity of shared memory (see section 4.6 “Shared Memory” on page 43)
- Processor clock frequency (see section 4.3 “PowerPC CPU” on page 40)
- Capacity of user flash (see section 4.8 “User Flash” on page 53)
- Capacity of L2 cache (see section 4.4 “L2 Cache” on page 41)
- PN15 connector (see section 3.7.3 “ISA Connector” on page 21)

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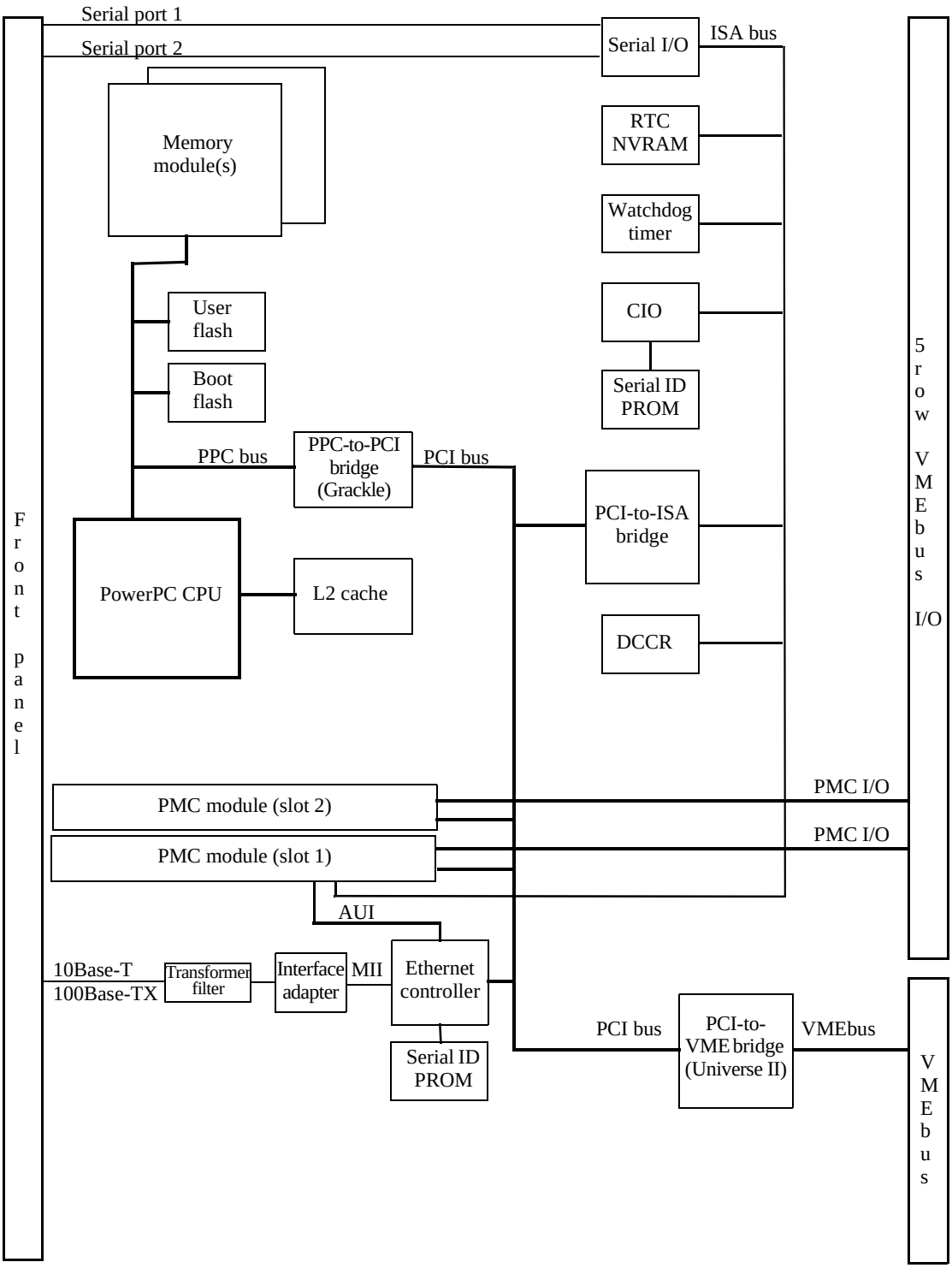
Figure 5 PPC/PowerCore-6750 Block Diagram



Bus Overview

The following table gives an overview of the different buses, their busmodes, and the connected devices.

Table 12 Buses, Busmodes, and Connected Devices

Bus	Busmode	Connected Devices
PPC bus	Big endian mode	PowerPC CPU Shared memory Boot flash User flash PPC-to-PCI bridge
PCI bus	Little endian mode	Ethernet controller PMC slots 1 and 2 PCI-to-VME bridge (Universe II) PPC-to-PCI bridge PCI-to-ISA bridge
VMEbus	Big endian mode	VME connectors P1 and P2 PCI-to-VME bridge (Universe II)
ISA bus	Little endian mode	CIO RTC/NVRAM Serial I/O ports 1 and 2 DRAM and cache configuration register (DCCR) PCI-to-ISA bridge

Bus Frequencies

The frequencies of the buses depend on the CPU type and its frequency. The following table shows the frequencies of the different buses:

Table 13 Bus Frequencies

CPU Type and Frequency	Bus Frequency [MHz]		
	ISA	PCI	PPC
PowerPC 750/233	8.25	33	66
PowerPC 750/300	8.25	33	82.5
PowerPC 750/400	8.25	33	82.5

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4.1 PPC/PowerCore-6750 Address Map

PPC/PowerCore-6750 provides a CHRP compliant address map. The following tables show the address map of PPC/PowerCore-6750:

- PPC/PowerCore-6750 Memory Map seen from the CPU (addresses on the processor bus)
- PPC/PowerCore-6750 Memory Map seen from the PCI (memory space addresses on the PCI bus)
- PPC/PowerCore-6750 I/O Map seen from the PCI (I/O space addresses on the PCI bus)
- PPC/PowerCore-6750 Configuration Base Addresses (configuration addresses for the on-board PCI devices)
- PPC/PowerCore-6750 ISA Bus Ports seen from the CPU (physical addresses for the on-board ISA devices)
- PPC/PowerCore-6750 PCI I/O Devices seen from the CPU (physical addresses for the on-board PCI I/O devices)

Note: **Before erasing or programming the boot flash ensure that you do not destroy the FORCE COMPUTERS PowerBoot boot image and make a copy of the boot flash device in socket J36 by using a programmer. Always remember the following access rule for any reserved bits in any PPC/PowerCore-6750 register: written as `0` read as undefined. All registers must be written or read using the data path width documented for the respective register.**

Table 14 PPC/PowerCore-6750 Memory Map seen from the CPU

Address on the PPC Bus	Device	Accessible Bus		Cache		Bus Width [bit]
		PCI	VME	L1	L2	
0000.0000_{16} … $3FFF.FFFF_{16}$	Shared memory space consisting of: • lower memory module • and upper memory module The memory space begins with bank 0 and is contiguous. The end address depends on the memory capacity.	Y	Y	Y	Y	[64]
4000.0000_{16} … $7FFF.FFFF_{16}$	reserved	–	–	–	–	–
8000.0000_{16} … $FCFF.FFFF_{16}$	PCI memory space VME memory	Y	Y	N	N	[32]
$FD00.0000_{16}$ … $FDFF.FFFF_{16}$	PCI/ISA memory space 0000.0000_{16} … $00FF.FFFF_{16}$ on PCI (see table 16 “PPC/PowerCore-6750 I/O Map seen from the PCI” on page 36)	Y	Y	N	N	[8]
$FE00.0000_{16}$ … $FE7F.FFFF_{16}$	ISA bus ports (see table 18 “PPC/PowerCore-6750 ISA Bus Ports seen from the CPU” on page 37)	Y	Y	N	N	[8]
$FE80.0000_{16}$ … $FEBF.FFFF_{16}$	PCI I/O space 0080.0000_{16} … $00BF.FFFF_{16}$ on PCI (see table 16 “PPC/PowerCore-6750 I/O Map seen from the PCI” on page 36)	Y	Y	N	N	[32]
$FEC0.0000_{16}$ … $FEDF.FFFF_{16}$	Configuration address register of the PPC-to-PCI bridge	Y	Y	N	N	[32]
$FEE0.0000_{16}$ … $FEEF.FFFF_{16}$	Configuration data register of the PPC-to-PCI bridge	N	N	N	N	[32]
$FEF0.0000_{16}$ … $FEFF.FFFF_{16}$	PCI interrupt acknowledge	N	N	N	N	[32]
$FF00.0000_{16}$ … $FFDF.FFFF_{16}$	reserved	–	–	–	–	–

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Table 14 PPC/PowerCore-6750 Memory Map seen from the CPU (cont.)

Address on the PPC Bus	Device	Accessible Bus		Cache		Bus Width [bit]
		PCI	VME	L1	L2	
$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$	User flash space	Y	Y	Y	Y	[8]
$FFF0.0000_{16}$ … $FFFF.FFFF_{16}$	Boot flash space	Y	Y	Y	Y	[8]

Table 15 PPC/PowerCore-6750 Memory Map seen from the PCI

PCI Memory Address	Device	Accessible Bus		Cache		Bus Width [bit]
		PPC	VME	L1	L2	
0000.0000_{16} … $3FFF.FFFF_{16}$	Shared memory space consisting of: Lower memory module Upper memory module The memory space begins with bank 0 and is contiguous. The end address depends on the memory capacity.	Y	Y	Y	Y	[64]
4000.0000_{16} … $7FFF.FFFF_{16}$	Reserved	–	–	–	–	–
8000.0000_{16} … $FCFF.FFFF_{16}$	PCI memory space VME memory space	Y	Y	N	N	[32]
$FD00.0000_{16}$ … $FDFF.FFFF_{16}$	Shared memory space 0000.0000_{16} ... $00FF.FFFF_{16}$ (see table 14 “PPC/PowerCore-6750 Memory Map seen from the CPU” on page 34)	Y	Y	N	N	[32]
$FE00.0000_{16}$ … $FFDF.FFFF_{16}$	Reserved	–	–	–	–	–
$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$	User flash space	Y	Y	Y	Y	[8]
$FFF0.0000_{16}$ … $FFFF.FFFF_{16}$	Boot flash space	Y	Y	Y	Y	[8]

Table 16 PPC/PowerCore-6750 I/O Map seen from the PCI

PCI I/O Address	Device	Accessible bus		Cache		Bus Width [bit]
		PPC	VME	L1	L2	
0000.0000_{16} … $0000.FFFF_{16}$	ISA I/O space $FE00.0000_{16}$ ... $FE00.FFFF_{16}$ on PowerPC CPU (see table 14 “PPC/PowerCore-6750 Memory Map seen from the CPU” on page 34)	Y	Y	N	N	[8]
0001.0000_{16} … $007F.FFFF_{16}$	Reserved	–	–	–	–	–
0080.0000_{16} … $00BF.FFFF_{16}$	PCI I/O space $FE80.0000_{16}$ ... $FEBF.FFFF_{16}$ on PowerPC CPU (see table 14 “PPC/PowerCore-6750 Memory Map seen from the CPU” on page 34)	Y	Y	N	N	[32]
$00C0.0000_{16}$ … $FFFF.FFFF_{16}$	Reserved	–	–	–	–	–

Table 17 PPC/PowerCore-6750 Configuration Base Addresses

Configuration Base Address	Device
8000.0000_{16}	Base address
$8000.C000_{16}$	Universe II
$8000.D000_{16}$	PCI-to-ISA bridge
$8000.D100_{16}$	PCI-to-ISA bridge (not supported)
$8000.D800_{16}$	Ethernet controller
$8000.E000_{16}$	PMC 1
$8000.E800_{16}$	PMC 2

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Table 18 **PPC/PowerCore-6750 ISA Bus Ports seen from the CPU**

Address	Device
$FE00.0073_{16}$	NVRAM/RTC address low register
$FE00.0074_{16}$	reserved
$FE00.0075_{16}$	NVRAM/RTC address high register
$FE00.0077_{16}$	NVRAM/RTC data register
$FE00.0300_{16}$ … $FE00.0303_{16}$	CIO registers
$FE00.0308_{16}$	DCCR
$FE00.03F8_{16}$ … $FE00.03FF_{16}$	Serial I/O port 1
$FE00.02F8_{16}$ … $FE00.02FF_{16}$	Serial I/O port 2

Table 19 **PPC/PowerCore-6750 PCI I/O Devices seen from the CPU**

Address	Device
$FE85.0000_{16}$ … $FE85.003F_{16}$	Ethernet controller
$FE81.0000_{16}$ … $FE81.0FFF_{16}$	PCI-to-VME bridge (Universe II)
user defined	PMC 1
user defined	PMC 2
$FEC0.0000_{16}$ … $FEDF.FFFF_{16}$	PCI configuration address register
$FEE0.0000_{16}$ … $FEEF.FFFF_{16}$	PCI configuration data register
$FEF0.0000_{16}$ … $FEFF.FFFF_{16}$	PCI interrupt acknowledge register

Note: **This address map is a default address map which can be changed by the user.**

4.2 PPC/PowerCore-6750 Interrupt Map

The PCI-to-ISA bridge monitors all PPC/PowerCore-6750 interrupt requests (IRQs):

Interrupt Requests

- Interrupt requests of all 4 PCI bus interrupt levels
- Interrupt requests from on-board ISA bus devices, e.g. from the serial controller
- Optional interrupt requests (see figure 2 “PN15 Connector Pinout” on page 22)
- Interrupt requests from the VMEbus interface

ACFAIL* and SYSFAIL*

Additionally, the VMEbus signals ACFAIL* and SYSFAIL* can be programmed in the PCI-to-VME bridge (Universe II) to assert PCI interrupt requests.

PCI-to-ISA Bridge Interrupt Controller

The PCI-to-ISA bridge provides an ISA compatible interrupt controller that incorporates the functionality of 2 interrupt controllers. The 2 controllers are cascaded so that 13 chip external and 3 chip internal interrupts are possible.
For information on programming the interrupt controller, read section 4.12.2 “Interrupt Controller” on page 70 and see “PCI-to-ISA Bridge – W83C553F”, *Data Sheets*.

Flexible Interrupt Programming

Every interrupt source, including the VMEbus IRQs, can be enabled and disabled to interrupt the CPU. The PCI-to-ISA bridge supplies the interrupt vectors for all interrupts except the NMI.

NMI

The NMI is routed from the IOCHK interrupt via the PPC-to-PCI bridge to the MCP# signal at the PowerPC CPU. The NMI has the highest priority and is a non-vectored processor exception.

Interrupt Priority

The following table shows the default mapping of the interrupts and their interrupt priority. Interrupt priority level 0 is the highest priority, level 15 is the lowest priority. The mapping of the interrupts and the interrupt priority can be set also by the user.

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Table 20 Default PPC/PowerCore-6750 Interrupt Map

Function	Device	PCI-to-ISA Bridge IRQ	Interrupt Priority Level
Watchdog timer/ abort key/SERR #	Dedicated logic	IOCHK (MCP)	0
Timer 1/counter 0	PCI-to-ISA bridge	IRQ0	1
User available	PN15 connector (factory option)	IRQ1	2
Cascade	PCI-to-ISA bridge	IRQ2	–
Serial port 2	Serial port 2	IRQ3	11
Serial port 1	Serial port 1	IRQ4	12
INTD #	PCI devices	IRQ5	13
User available	PN15 connector (factory option)	IRQ6	14
User available	PN15 connector (factory option)	IRQ7	15
Timer/parallel port IRQ	CIO	IRQ8#	3
reserved	–	IRQ9	4
INTA #	PCI device: Ethernet controller	IRQ10	5
INTB #	PCI device: Universe II	IRQ11	6
User available	PN15 connector (factory option)	IRQ12	7
reserved	–	IRQ13	8
INTC #	PCI devices	IRQ14	9
reserved	–	IRQ15	10

The following table shows the interrupt routing of the PMC slots.

Table 21 PMC Interrupt Routing

Interrupt Lines		
PCI-to-ISA Bridge	**PMC slot 1**	**PMC slot 2**
INTA #	INTC #	INTB #
INTB #	INTD #	INTC #
INTC #	INTA #	INTD #
INTD #	INTB #	INTA #

4.3 PowerPC CPU

The microprocessor PowerPC 750 is one of the basic components of the PPC/PowerCore-6750.
For detailed information, refer to the *PowerPC Instruction Set* available from Motorola Semiconductors.

The PowerPC 750 consists of a processor core and an internal L2 tag combined with a dedicated L2 cache interface and a PPC bus. It provides:

- 32-bit effective addresses
- Integer data types of 8, 16, and 32 bits
- Floating-point data types of 32 and 64 bits

Execution Units

The PowerPC 750 is a superscalar processor sustaining a peak throughput of 3 instructions per clock. It includes the following independent execution units:

- Control unit
- Floating-point unit
- Two fixed-point units
- Load and store unit
- Cache and memory unit
- Bus interface unit

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Additional Features

- 32-KByte L1 data cache
- 32-KByte L1 instruction cache
- Up to 1-MByte L2 cache
- Memory management unit (MMU) with 128 entries, two-way set-associative instruction TLB with 128 entries, two-way set-associative data TLB

4.4 L2 Cache

PPC/PowerCore-6750 provides an L2 cache of up to 1 MByte. The L2 cache is controlled by the L2 cache controller of the PowerPC 750. The L2 tag is 2 way set-associative with 4-K entry tags per way. Only the memory space of the processor bus devices can be cached in the L2 cache.

Data Sheet

For further information on programming the L2 cache controller, see the respective *PowerPC Instruction Set* available from Motorola Semiconductors.

L2 Cache Size

The available size of the L2 cache can be read by the software from the DCCR, bits [7...6].

Table 22 DCCR, Bits [7…6]

FE00.0308$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	DCCR [7…6]		DCCR [5…0]					

DCCR [7…6] DCCR [7…6] indicate the L2 cache configuration.

= 00_2 No L2 cache available

= 01_2 256-KByte L2 cache

= 11_2 512-KByte L2 cache

= 10_2 1-MByte L2 cache

DCCR [5…0] see table 24 “DCCR, Bits [5…0]” on page 46

4.5 Watchdog Timer

The watchdog timer installed on PPC/PowerCore-6750 monitors the CPU activity. The watchdog timer is able to:

- Issue an NMI to the PowerPC CPU after the first timeout period
- Generate a reset pulse after a second timeout period

4.5.1 Watchdog Operation

The watchdog timer monitors the PowerPC CPU activity by awaiting a trigger event from the PowerPC CPU within the timeout period.

Trigger Event

The bit TRWD in the CIO port C data register starts the watchdog and controls whether the watchdog timer is triggered.

Table 23 CIO Port C Data Register, Bit [3…2]

$FE00.0300_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	used as masking bits for write accesses to bit 3…0 (e.g.: if bit 4 is set to 1, bit 0 cannot be written)				WDNMI	TRWD	LED[1…0]	

WDNMI (R)

WDNMI indicates whether the watchdog timer has generated an NMI. When the watchdog timer is retriggered, WDNMI will be cleared.

= 0 no NMI has been generated by the watchdog timer.

= 1 NMI has been generated by the watchdog timer.

If the retriggering does not occur within the second watchdog timeout period after generating the NMI, the watchdog timer generates a reset pulse. By this, the watchdog timer automatically stops itself. In this case it must be restarted by resetting TRWD.

TRWD

TRWD starts the watchdog timer. A positive edge at this pin retriggers the watchdog.

= 0 watchdog timer is started, if low level is held for more than 8 ms.

0 → 1 watchdog timer is retriggered.

= 1 no change (default)

LED[1…0]

see table 42 “CIO Port C Data Register” on page 75

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Timeout	A set of watchdog timeout periods can be selected via SW5-2 (see table 8 “Default Switch Settings” on page 16).
Enable the Watchdog	The watchdog is enabled by setting SW5-1 to ON (default “OFF”, see page 16).
Start the Watchdog	When the watchdog is started, it cannot be stopped unless a reset occurs. In case of a reset the watchdog timer is automatically disabled.
Retrigger the Watchdog	The watchdog is retriggered, if a positive edge occurs at the `TRWD` signal. This means that you have to write `0` to `TRWD`, followed by `1`.
Interrupt	The watchdog interrupt is the IOCHCK input of the PCI-to-ISA bridge, which is routed to the MCP interrupt input of the PowerPC CPU. This interrupt is called NMI.
NMI Generation	If the retrigger event does not occur within the first watchdog timeout period, the watchdog timer generates an NMI to the PowerPC CPU. If the retrigger event occurs within the second watchdog timeout period after generating the NMI, the watchdog timer is restarted.

4.6 Shared Memory

Per default the shared memory of the CPU board is provided by one (lower) memory module directly located on the CPU board. Depending on the (lower) memory module, which is per default installed on the CPU board, the capacity of the shared memory may be increased by installing an upper memory module on top of the lower one.

Requirements	For detailed information on requirements, qualified configurations, and max. power consumption of the memory modules, see section 3.1 “Installation Prerequisites and Requirements” on page 10.
Installation	For information on installing the memory module, refer to the respective *Memory Module Installation Guide*.

Accessibility

The shared memory is accessible from:

- PowerPC CPU,
- Universe II DMA controller,
- Other VMEbus masters,
- Ethernet DMA controller,
- Other PCI DMA controllers on PMC modules,
- PCI-to-ISA bridge DMA controller.

ECC

- If an EDO DRAM memory module is installed, only ECC is supported.
- If an SDRAM memory module is installed, neither ECC nor parity is supported.

The ECC detects and corrects all single-bit errors. Double-bit errors and errors within a nibble are only detected but not corrected. ECC is enabled per default and can be disabled by the software (see “PPC-to-PCI Bridge – MPC106 (Grackle)”, *Data Sheets*).

Shared Memory Accesses

The following two different types of shared memory accesses are possible:

1. Shared memory access without ECC:
   - In case of shared memory read accesses the bytes requested by the master are read from the shared memory without additional transfers for ECC. If less than one long-word is read, the extraneous data is ignored by the PPC-to-PCI bridge.
   - In case of shared memory write accesses the bytes provided by the master are written into the shared memory without additional transfers for ECC. If less than one long-word is written, the extraneous data is masked by control signals. Therefore, only targeted bytes are written actually.
2. Shared memory accesses with ECC:
   - A shared memory read access to less than one long-word is performed by the PPC-to-PCI bridge as a read access to one aligned long-word, so that the ECC byte can be checked. The 8 bytes and the ECC byte are stored in the memory controller.
   - A shared memory write access to less than one long-word is performed by the PPC-to-PCI bridge as a read-modify-write access to one aligned long-word. The PPC-to-PCI bridge reads the aligned long-word, checks the ECC byte, and merges the written data with the data read from the shared memory. Then the PPC-to-PCI bridge

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generates a new ECC for the merged long-word and writes the long-word and ECC code into the shared memory.

4.6.1 Memory controller

The memory controller is located in the PPC-to-PCI bridge.

Shared Memory Configuration

The memory controller registers of the PPC-to-PCI bridge are accessible via the configuration address register (CAR) and the configuration data register (CDR). For configuring the memory controller, the CAR and the CDR must be set appropriately (see section 4.9 “PPC-to-PCI Bridge” on page 56).

4.6.2 Shared Memory Performance

The shared memory control logic is optimized for fast accesses from the PowerPC CPU providing the maximum performance with enabled ECC. Since the PowerPC CPU includes an on-chip data and instruction cache many CPU accesses are cache line "burst fills". Within four 8-byte cycles these burst fills attempt to read 32 consecutive bytes into the PowerPC CPU.

EDO DRAM shared memory

"8-4-4-4" Burst Transfer

If an EDO DRAM memory module is installed, the first read cycle of such a burst usually requires 8 PPC bus clock cycles. Due to the optimized design of the memory control logic, each subsequent cycle requires only 4 PPC bus clock cycles to complete. This is commonly called an "8-4-4-4" burst transfer. Overall, the total cache line "burst fill" operation requires 20 PPC bus clock cycles to transfer 32 bytes providing a maximum memory bandwidth of over 105 MByte/s at 66-MHz PPC clock frequency.

Single Read and Write

Not all CPU accesses are burst transfers. Single read and write transactions are also supported at maximum speed. A single read or write access (1, 2, 4, or 8 bytes) requires 7 PPC bus-clock cycles. Distributed asynchronous refresh is provided every 14 µs and an access during a pending refresh cycle may be delayed by a maximum of six additional clock cycles at 66-MHz PPC clock frequency.

SDRAM shared memory

"3-1-1-1" Burst Transfer

Compared with an EDO DRAM shared memory the performance increases significantly if an SDRAM memory module is installed. The first read cycle of a burst usually requires three PPC bus clock cycles. Due to

the optimized design of the memory control logic, each subsequent cycle requires only 1 PPC bus clock cycle to complete. This is commonly called a "3-1-1-1" burst transfer. Overall, the total cache line "burst fill" operation requires 6 PPC bus clock cycles to transfer 32 bytes providing a maximum memory bandwidth of 440 MByte/s at 82.5-MHz PPC clock frequency

Single Read and Write

A single read or write access (1, 2, 4, or 8 bytes) requires 4 PPC bus-clock cycles. Distributed asynchronous refresh is provided every 14.5 µs and an access during a pending refresh cycle may be delayed by a maximum of eight additional clock cycles at 82.5-MHz PPC clock frequency.

4.6.3 Shared Memory Capacity

The capacity of the shared memory is encoded in the DCCR.

Table 24 DCCR, Bits [5…0]

FE00.0308$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	DCCR [7…6]		DCCR [5…0]					

DCCR [7…6] see table 22 “DCCR, Bits [7…6]” on page 41

DCCR [5…0] DCCR [5…0] indicate the capacity of the installed shared memory. All combinations not listed in the following table are reserved.

Table 25 EDO DRAM Capacity

DCCR [5…0]						**Capacity [MByte]**	
Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Lower EDO DRAM Mem. Module**	**Upper EDO DRAM Mem. Module**
don’t care	don’t care	0	1	1	1	16	–
don’t care	don’t care	1	1	0	1	64	–
don’t care	don’t care	1	0	0	1	64	128

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Table 26 SDRAM capaCity

DCCR [5…0]						Capacity [MByte]	
Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Lower SDRAM Mem. Module**	**Upper SDRAM Mem. Module**
don't care	don't care	0	0	1	1	64	–
don't care	don't care	0	0	0	1	128	–
don't care	don't care	0	0	1	0	64	128
don't care	don't care	0	0	0	0	128	128

4.6.4 Shared Memory Organization

The EDO DRAM is arranged in one or three memory banks with nine 2M * 8 or 8M * 8 EDO DRAM devices in each bank.
The SDRAM is arranged in one, three, or four banks with eight 8M * 8 SDRAM devices in each bank.
Each memory module bank is 64-bit wide. The EDO DRAM memory banks provide one additional byte for the ECC.

4.6.5 Cache Coherency and Snooping

To maintain the cache coherency of the shared memory the PowerPC CPU has the capability of snooping. On a snooped external bus cycle the PowerPC CPU invalidates the cache line that is hit. Snoop hits invalidate the cache line in all cases (also for alternate master read/write cycles).

Note: **To guarantee the cache coherency of the shared memory, the snooping in the processor interface configuration register of the PPC-to-PCI bridge has to be enabled (see "PPC-to-PCI Bridge – MPC106 (Grackle)",** ***Data Sheets*****).**

4.6.6 Shared Memory Access from the PowerPC CPU

After initialization the firmware enables the complete shared memory at start address 0000.0000_{16}. The shared memory address range, which is accessible via the PPC bus, can be programmed in the PPC-to-PCI bridge memory controller. Depending on the capacity of the shared mem-

ory, the end address is set to the maximum available shared memory by the firmware.

Memory Modules

For information on the contiguousness of the shared memory space, see table 14 “PPC/PowerCore-6750 Memory Map seen from the CPU” on page 34.

Table 27 Shared Memory Access Address Ranges from the PowerPC CPU

Address Range	Capacity of the Lower Mem. Mod. [MByte]	Capacity of the Upper Mem. Mod. [MByte]
0000.0000_{16} …$00FF.FFFF_{16}$	16	0
0000.0000_{16} …$03FF.FFFF_{16}$	64	0
0000.0000_{16} … $07FF.FFFF_{16}$	128	0
0000.0000_{16} … $0BFF.FFFF_{16}$	64	128
0000.0000_{16} … $0FFF.FFFF_{16}$	128	128

4.6.7 Shared Memory Access via VMEbus

Shared memory access from or to the VMEbus is routed by Universe II via the PCI bus and the PPC-to-PCI bridge. The start and end access addresses can be programmed.

Programmable Access Address Range

The access address of the shared memory for other VMEbus masters is programmable via Universe II. Both the start and the end address of the shared memory are Universe II programmable in 4-KByte increments (see “PCI-to-VME bridge – Universe II”, *Data Sheets*). Therefore, the address range used by other VMEbus masters is not necessarily the same as the one used by the PowerPC CPU for local accesses.

Write Protection

The write protection of the programmed shared memory range depends on the VMEbus address modifier codes: For example, in privileged mode the shared memory can be read and written, while in non-privileged mode the shared memory can only be read, or a non-privileged access can be prohibited altogether.

VMEbus Access Cycle

When Universe II detects a VMEbus access cycle to the programmed address range of the shared memory, it requests bus mastership of the PCI bus via the PCI bus arbiter. After the arbiter has granted the PCI bus

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mastership to Universe II, the VMEbus access cycle is executed and all data is latched from (read cycles) or stored to (write cycles) the shared memory. After this the cycle is terminated and Universe II keeps the PCI bus mastership until another PCI bus master requests the bus. Universe II also completes the fully asynchronous VMEbus access cycle.

Locked Read-Modify-write Cycles

Read-modify-write cycles from the VMEbus are indivisible. Locked PCI bus cycles achieve that Universe II retains the local bus mastership until the VMEbus cycle is finished. By this no other local bus master (PowerPC CPU) will access the shared memory location before the VMEbus cycle is terminated.

4.6.8 Shared Memory Access from the Ethernet Controller

The Ethernet controller uses the PCI bus mastership to transfer commands, data, and status information to and from the shared memory via the PCI bus and the PPC-to-PCI bridge.

4.6.9 Shared Memory Access from PMC Modules

The PMC modules may use the PCI bus mastership to transfer commands, data, and status information to and from the shared memory via the PCI bus and the PPC-to-PCI bridge.

4.6.10 Shared Memory Access from the PCI-to-ISA Bridge

The PCI-to-ISA bridge uses the PCI bus mastership to transfer commands, data, and status information to and from the shared memory via the PCI bus and the PPC-to-PCI bridge.

4.7 Boot Flash

Since the flash memory area is located on the PPC bus, the reset vector table in the boot flash is visible to the CPU after power-on reset before any initialisation by the software. A memory address range of 2 MByte is available for the complete flash memory, i.e. for the user flash and the boot flash (see section 4.8 “User Flash” on page 53). For the boot flash the first 1-MByte range is used. If more than 1 MByte is installed, the boot flash is visible bankwise, each bank consisting of 1 MByte. Since only 1 MByte is preserved for the boot flash bank, one additional parallel port pin provides switching techniques (see table 28 “CIO Port A Data Register, Bits [7] and [4]” on page 50) to increase the boot flash capacity.

4.7.1 Boot Flash Address Range

The flash memory area is 8-bit wide organized. The PPC-to-PCI bridge provides 21 addressing lines to address the board flash memory. Therefore 2 MByte of the complete flash address range FFE0.0000$_{16}$ ... FFFF.FFFF$_{16}$ are accessible for 8-bit wide organized flash devices. 1 MByte of the address space is used for the boot flash.

The following register map shows the bits provided to achieve the maximum of 2-MByte boot flash. The boot flash consists of one device with a maximum of two banks each consisting of 1 MByte.

Table 28 CIO Port A Data Register, Bits [7] and [4]

FE00.0302								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	VPP_CTRL	ISA_IDENT	reserved	BOOT_A20	FLSH_SEL[1…0]		reserved	USER_A20

VPP_CTRL (R/W) VPP_CTRL controls whether the +12V programming voltage V_{PP} for the boot flash and user flash is ON.

= 0 V_{PP} is turned off.

= 1 V_{PP} is turned on.

ISA_IDENT (R) see table 45 “CIO Port A Data Register, Bit [6]” on page 79

BOOT_A20 (R/W) BOOT_A20 distinguishes between the 1 MByte boot flash areas of a single device. The output of BOOT_A20 is connected to the address pin A20 of the boot flash TSOP footprint via a programmable logic device. Since the boot flash can be accessed only in the address range FFF0.0000$_{16}$...FFFF.FFFF$_{16}$, the software has to set this bit appropriately to select the considered 1 MByte bank. The default setting of BOOT_A20 is 0. This bit extends the PPC-to-PCI bridge addressing

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lines. This bit should not be changed by processor instructions fetched from the boot flash device.

Table 29 Boot Flash Address Range

Address Range	Boot Flash Address Space	Extended Boot Flash Capacity via BOOT_A20
$FFF0.0000_{16}$ … $FFF7.FFFF_{16}$	512 KByte	512 KByte
$FFF0.0000_{16}$ … $FFFF.FFFF_{16}$	1 MByte	1 MByte
$FFF0.0000_{16}$ … $FFFF.FFFF_{16}$	1 MByte	2 MByte

FLSH_SEL [1…0] (R/W) — see table 32 “CIO Port A Data Register, Bits [7], [3…2], and [0]” on page 54

USER_A20 (R/W) — see table 32 “CIO Port A Data Register, Bits [7], [3…2], and [0]” on page 54

Note: **The firmware supports commands to select the device bank which is to be mapped into the address range (see *PowerBoot Instruction Set,* section "FSELECT – Selecting Flash Memory").**

Reset Vector — The CPU reset vector is located at $FFF0.0100_{16}$.

4.7.2 Boot Flash Size and Address Map

Caution

The boot flash size of the PLCC devices is a factory option. Do not reduce or increase the size of the boot flash devices even if socketed. Otherwise the devices and/or data could be damaged.
The accessible address range of the boot flash is determined by the boot flash capacity. Therefore, the address range depends on the CPU board type.

Table 30 Boot Flash Address Map

Boot flash		**Total Boot Flash Capacity**	**Resulting Address Range for Processor Instructions**	**Bank address via `BOOT_A20`**
J41 TSOP device	**J36** PLCC device			
1 MByte	–	1 MByte	`FFF0.0000`$_{16}$ … `FFFF.FFFF`$_{16}$	`0`
2 MByte	–	2 MByte	`FFF0.0000`$_{16}$ … `FFFF.FFFF`$_{16}$	`0…1`
–	512 KByte	512 KByte	`FFF0.0000`$_{16}$ … `FFF7.FFFF`$_{16}$	`0`

4.7.3 Boot Flash Devices

The CPU board provides one user programmable boot flash device at one of the following locations.

Location J41 (unsocketed) or J36 (socketed)

Base Address `FFF0.0000`$_{16}$

Device Types The following two types of boot flash devices are available (factory option):

- Boot flash devices programmable at VPP = 12 V
- Boot flash devices programmable at VPP = 5 V

The following table shows the boot flash factory options using the listed device types (or equivalent).

Table 31 Boot flash factory options, device types, and default configuration

	Device Type	**Package Type**	**Default**
1.	29F040:512K * 8 VPP: 5V	PLCC (socketed at J36)	x
2.	28F008:1M * 8 VPP: 12V	TSOP (unsocketed at J41)	
3.	29F016:2M * 8 VPP: 5V	TSOP (unsocketed at J41)	

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4.7.4 Programming the Boot Flash

Writing to the boot flash is only enabled if SW6-4 is set to ON (default "OFF", see page 16). The programming voltage for the flash devices is turned on by setting bit 7 of the CIO port A data register appropriately (see table 28 "CIO Port A Data Register, Bits [7] and [4]" on page 50).

When writing to the boot flash is enabled, programming is handled correctly by PowerBoot packaged with PPC/PowerCore-6750 (see PowerBoot *Instruction Set* "FERASE – Erasing Flash Memories" and "FPROG – Programming Flash Memories") and by the assembly process.

Caution

Before erasing or programming the boot flash ensure that you do not destroy FORCE COMPUTERS' firmware and make a copy of the boot flash contents.

4.8 User Flash

The second MByte of the flash memory space is used for the user flash. If more than 1-MByte user flash is installed, the user flash is visible only bankwise, each bank consisting of 1 MByte. Since only 1 MByte is preserved for the user flash bank, three additional parallel port pins (see table 28 "CIO Port A Data Register, Bits [7] and [4]" on page 50) provide switching techniques to increase the user flash capacity. These pins extend the PPC-to-PCI bridge addressing lines.

4.8.1 User Flash Address Range

The flash memory area is 8-bit wide organized. The PPC-to-PCI bridge provides 21 addressing lines to address the flash memory. Therefore 2 MByte of the complete flash address range $\texttt{FFE0.0000}_{16}$ ... $\texttt{FFFF.FFFF}_{16}$ are accessible for 8-bit wide organized flash devices. The second 1 MByte range is used for the user flash.

The following table shows the additional bits to be added to achieve the maximum of 8-MByte user flash. The user flash can be divided into four flash devices each consisting of two banks with 1 MByte. CIO port A holds these additional bits.

Table 32 CIO Port A Data Register, Bits [7], [3…2], and [0]

FE00.0302								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	VPP_CTRL	ISA_IDENT	reserved	BOOT_A20	FLSH_SEL[1…0]		reserved	USER_A20

VPP_CTRL (R/W) VPP_CTRL controls whether the +12V programming voltage V_{PP} for the boot flash and user flash is ON.

= 0 V_{PP} is turned off.

= 1 V_{PP} is turned on.

ISA_IDENT (R) see table 45 “CIO Port A Data Register, Bit [6]” on page 79

BOOT_A20 (R/W) see table 28 “CIO Port A Data Register, Bits [7] and [4]” on page 50

FLSH_SEL [1…0] (R/W) FLSH_SEL[1…0] selects the user flash device which is paged into the memory range $FFE0.0000_{16}$ … $FFEF.FFFF_{16}$.

Table 33 User Flash Address Map

User Flash	FLSH_SEL [1…0]	Address Range
1	00_2	$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$
2	01_2	$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$
3	10_2	$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$
4	11_2	$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$

USER_A20 (R/W) USER_A20 distinguishes between the 1 MByte user flash areas of a single device. The output of USER_A20 is directly connected to the address pin A20 of the user flash footprints. Since the user flash can be accessed only in the address range $FFE0.0000_{16}$…$FFEF.FFFF_{16}$, the software

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has to set this bit appropriately to select the considered 1 MByte bank of the related device.

Table 34 User Flash Address Range

Address Range	User Flash Address Space	Extended User Flash Capacity via USER_A20
$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$	1 MByte	1 MByte
$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$	1 MByte	2 MByte

Note: **The firmware supports commands to select the device bank which is to be mapped into the address range (see *PowerBoot Instruction Set,* section "FSELECT – Selecting Flash Memory").**

4.8.2 User Flash Size

The following user flash capacities are available:

- 0 MByte
- 4 MByte if
  - four 1M * 8 devices
  - or two 2M * 8 devices are used
- 8 MByte if four 2M * 8 devices are used

4.8.3 User Flash Devices

The user flash consists of up to 4 user programmable flash devices.

Base Address $FFE0.0000_{16}$

Configurations Three user flash configurations are available as factory options:

- No user flash devices
- 1M * 8 user flash devices
- 2M * 8 user flash devices

The following table shows the factory options available for the user flash using the device types listed (or equivalent). The default configuration of the board depends on its frequency:

- For the 233-MHz board the second option is the default configuration.
- For the boards with processor clock frequency of 300 MHz and higher the third option is the default configuration

Table 35 User Flash Factory Options and Device Types

	Device Type	Address Range
1.	No user flash installed	
2.	28F008:1M * 8 VPP: 12V	$\texttt{FFE0.0000}_{16}$ … $\texttt{FFEF.FFFF}_{16}$
3.	29F016:2M * 8 VPP: 5V	$\texttt{FFE0.0000}_{16}$ … $\texttt{FFEF.FFFF}_{16}$

4.8.4 Programming the User Flash

Writing to the user flash is only enabled if SW6-3 is set appropriately (default “OFF”, see page 16). The programming voltage for the user flash devices is turned on by setting bit 7 of the CIO port A data register appropriately (see table 32 “CIO Port A Data Register, Bits [7], [3…2], and [0]” on page 54).

When writing to the user flash is enabled, programming is handled correctly by PowerBoot packaged with PPC/PowerCore-6750 (see PowerBoot *Instruction Set* section “FERASE – Erasing Flash Memories” and section “FPROG – Programming Flash Memories”) and by the assembly process.

4.9 PPC-to-PCI Bridge

The PPC-to-PCI bridge provides an integrated and PowerPC compliant interface between the PowerPC CPU, the shared memory, the user flash and boot flash, and the PCI bus.

Processor Interface

The processor interface provides a 64-bit data bus and a 32-bit address bus. It supports full memory coherency. Furthermore, it pipelines processor accesses.

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Memory Interface

The memory interface is programmed to support the memory module(s) installed on the CPU board. The memory interface provides a 64-bit data bus to the memory module(s). Depending on the memory module ECC or parity is per default enabled by the software (see section 4.6 “Shared Memory” on page 43).The PPC-to-PCI bridge supports up to 1-Gbyte memory module(s).
The memory interface supports writing of flash memory and write buffering for PCI and processor accesses.

Features of the PCI Interface

The PCI interface implements the following features:

- Compliant with PCI 2.1
- Operation at 33 MHz
- PCI interlocked accesses to shared memory via lock pin and lock protocol
- Accesses to all PCI address spaces
- Selectable big or little endian operation
- Store gathering of PPC-to-PCI writes and PCI-to-memory writes and memory prefetching of PCI read accesses
- PCI configuration registers
- Data buffering (in/out)
- Parity support

Miscellaneous Features

Furthermore, the PCI interface provides the following features:

- Error reporting mechanism
- JTAG boundary scan
- Concurrent transactions on the processor and the PCI bus

Registers

The register set of the PPC-to-PCI bridge is accessible via the configuration address register (CAR) and the configuration data register (CDR). To configure the memory controller, the CAR and the CDR must be set appropriately:

- To access the register set of the PPC-to-PCI bridge with offset `xy`, the CAR must contain $\texttt{xy00.0080}_{16}$ (see table 17 “PPC/PowerCore-6750 Configuration Base Addresses” on page 36). The register offset `xy` has to be written into the most significant byte of the CAR. The least significant byte must be set to 80_{16} (swapped byte).
- The CDR contains the contents for the memory controller registers (R/W) to be accessed.

Table 36 CAR and CDR Address Map

Register	Address
CAR	$FEC0.0000_{16}$
CDR	$FEE0.0000_{16}$

Example

If you want to enable memory bank 0 and 1, you have to access the memory bank, enable register at offset $A0_{16}$, and to write the value 03_{16} into this register (see “PPC-to-PCI Bridge – MPC106 (Grackle)”, *Data Sheets*):

1. Write the value $A000.0080_{16}$ to the CAR address $FEC0.0000_{16}$.
2. Write the value 03_{16} to the CDR address $FEE0.0000_{16}$.

Data Sheet

For a detailed description of configuring the memory controller, see “PPC-to-PCI Bridge – MPC106 (Grackle)”, *Data Sheets*.

4.10 PCI-to-VME Bridge – Universe II

The VMEbus interface of the PPC/PowerCore-6750 is realized via Universe II, a PCI-to-VME bridge. It acts as master and slave in the VMEbus system and is particularly convenient for PCI local bus systems.
For information on installation prerequisites and requirements, see section 3.1 “Installation Prerequisites and Requirements” on page 10.

Features

Universe II provides:

- Fully PCI compliant up to 33-MHz PCI bus interface
- Fully ANSI/VITA 1-1994 compliant 64-bit VMEbus interface
- Integral FIFOs for write posting to maximize bandwidth utilization (64 bits wide, 32 entries deep)
- Programmable DMA controller with linked list support
- Complete suite of VMEbus address and data transfer modes:
  - A32/A24/A16 master and slave
  - D64 (MBLT)/D32/D16/D08 master and slave
  - BLT, ADOH, RMW, LOCK
- Flexible register set, programmable from both the PCI bus and the VMEbus
- Full VMEbus system controller functionality

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- Four 32-bit mailboxes for interrupt generation on either bus
- Location monitor for interrupts and message passing
- Seven VME software interrupts
- Two semaphore registers to control access to system resources,
- IEEE 1149.1 JTAG testability support

CSR Base Address

The CSR base address is located at address $\texttt{FE81.0000}_{16}$.

Data Sheet

For a detailed description see “PCI-to-VME bridge – Universe II”, *Data Sheets*.

4.10.1 VMEbus Interface Overview

This section gives only a short overview of the VMEbus interface features. The following sections describe the VMEbus interface in detail.

ANSI/VITA Compliance

PPC/PowerCore-6750 provides a complete VMEbus interface compliant with ANSI/VITA 1-1994.

Supported Transfers

The VMEbus interface supports 64-bit (MBLT), 32-bit, 16-bit, and 8-bit data transfers, as well as unaligned data transfers (UAT). The extended, standard, and short I/O address modifier codes are implemented.

RMW Cycles

Read-modify-write cycles on the VMEbus (RMW cycles) are also supported. The address strobe signal is held low during RMW cycles while the data strobe signals are driven low twice, once for the read cycle and once for the write cycle, and high between both of them.

Interrupt Handler

The complete VMEbus interrupt management is done by Universe II enabling the use of a high-end multiprocessor board with distributed interrupt handling. Universe II acts as D08(O) interrupt handler in compliance with ANSI-VITA 1-1994, i.e. 8-bit interrupt vectors are supported, whereas 16-bit interrupt vectors are not supported.

All seven VMEbus interrupt requests (IRQs signals) are connected to the interrupt handling logic of Universe II.

- All seven VMEbus IRQ signals can be separately enabled or disabled.
- Every VMEbus interrupt request level causes a PCI interrupt (INTB#) if enabled.

Slot-1 Function

An arbiter with several arbitration modes and release functions is implemented with all slot-1 system controller functions (see section 4.10.6 “VMEbus Slot-1 Functions” on page 63):

- VMEbus arbiter
- SYSCLK driver
- IACK daisy chain driver

IACK Daisy Chain Driver

The CPU board includes an IACK daisy chain driver.

- If the CPU board is plugged in slot 1 and SW7-1 and SW7-2 are set accordingly, the CPU board acts as IACK daisy chain driver.
- If the CPU board is plugged in any other slot, the IACKIN-IACKOUT path will be closed.

4.10.2 VMEbus Master Interface

PCI Images

Universe II transfers data to the VMEbus within a maximum of eight programmed PCI slave images. Each image can be enabled or disabled independently. Posted write accesses are also programmable.

Access Address

The VMEbus access address is programmable via Universe II. Both the start and the end address of the accessible VMEbus address range are programmable in 4-KByte or 64-KByte increments.

Data Transfer Size

The VMEbus master interface supports all 32 data lines. It supports 64-bit (MBLT), 32-bit, 16-bit, and 8-bit data transfers as well as unaligned data transfers (UAT) and read-modify-write transfers.

The VMEbus address range is the largest part of the address map (see section 4.1 “PPC/PowerCore-6750 Address Map” on page 33). Universe II maps the PCI bus transaction to the maximum programmed VMEbus data width. According to this data width data are packed or unpacked.

Table 37 VMEbus Master Transfer Cycles Def. for Data Bus Width D32

Transfer Type	D31…24	D23…16	D15…08	D07…00
Byte on odd address Byte on even address			 x	x
Word			x	x
Long-word	x	x	x	x

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Table 37 **VMEbus Master Transfer Cycles Def. for Data Bus Width D32**

Transfer Type	D31…24	D23…16	D15…08	D07…00
Unaligned word		x	x	
Unaligned long-word A	x	x	x	
Unaligned long-word B		x	x	x
Read-modify-write				
byte on odd address				x
byte on even address			x	
word			x	x
long-word	x	x	x	x

Table 38 **VMEbus Master Transfer Cycles Defined for Data Bus Width D16**

Transfer Type	D31…24	D23…16	D15…08	D07…00
Byte on odd address				x
Byte on even address			x	
Word			x	x
Read-modify-write				
byte on odd address				x
byte on even address			x	
word			x	x

Access Modes

For VMEbus master access A32/A24/A16 accesses and CR/CSR accesses are allowed. Single-cycle transfers or block transfers are programmable.
Universe II allows data and program accesses in the privileged (supervisor) or non-privileged (user) mode. Additionally, Universe II supports 2 user defined address modifier codes. Every access mode (address modifier) can be separately enabled or disabled within the PCI slave image.

4.10.3 VMEbus Slave Interface

Slave Images — Within a maximum of eight programmed VMEbus slave images Universe II can be accessed from the VMEbus. Every image can be enabled or disabled independently. Prefetched read accesses and posted write accesses are also programmable.

Access Address — The access address of the shared memory for other VMEbus masters is programmable via Universe II. Both the start and the end address of the shared memory are programmable in 4-KByte or 64-KByte increments.

Data Transfer Size — The VMEbus slave interface for the shared memory supports all 32 data lines. It supports 64-bit (MBLT), 32-bit, 16-bit, and 8-bit data transfers as well as unaligned data transfers (UAT), and read-modify-write transfers.

Access Modes — For VMEbus slave access to the shared memory, A32/A24/A16 and CR/CSR accesses are allowed.
Universe II allows accesses in the privileged (supervisor) or non-privileged (user) mode for both data and program accesses. Additionally Universe II provides support for 2 user defined Address Modifier Codes. Each access mode can (address modifier) be separately enabled or disabled within the slave images.

4.10.4 DMA-Controller

Universe II uses a DMA controller for high-performance data transfer between the PCI bus and the VMEbus. Source, destination, length of transfer, and transfer protocol are programmable in several registers of Universe II.

Direct or Linked list DMA — The DMA controller can be set to one of the following modes:

- Direct DMA: In direct DMA mode the DMA registers are programmed directly by software
- Linked list DMA: In linked list mode Universe II loads the registers from the shared memory. The block of the shared memory containing the values for the DMA registers is called command packet. The command packets may be linked. If all linked command packets are executed, the DMA is complete.

16-Entry FIFO — For increased performance the DMA uses a 16-entry deep, 64-bit wide bidirectional FIFO.

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4.10.5 Exception Signals

SYSFAIL*, SYSRESET*, and ACFAIL* signal exceptions or status. These signals are connected to the CPU board via buffers, switches, and Universe II.

SYSRESET* Input

The VMEbus SYSRESET* signal is monitored by the CPU board only if SW5-3 is set to OFF (default “OFF”, see page 16).

SYSRESET* Output

A SYSRESET* is generated by PPC/PowerCore-6750 if SW7-4 is set to OFF (default “OFF”, see page 17). The reason for the SYSRESET* generation may be one of the following:

- Front-panel reset key is active
- SW_SYSRESET bit is set in the MISC_CTL register of the Universe II
- Watchdog timer generates a reset
- Power-up occurs
- Voltage sensor detects a low voltage on-board

SYSFAIL*

Universe II can be programmed to generate local interrupts when the SYSFAIL* signal is active.

ACFAIL*

The ACFAIL* line can be mapped to a PCI interrupt (INTB#). The CPU board can never drive the ACFAIL* signal.

4.10.6 VMEbus Slot-1 Functions

PPC/PowerCore-6750 may be used as system controller when the CPU board is plugged into slot 1 or when it is forced to be slot-1 device by appropriate setting of SW7-1 and SW7-2. Per default PPC/PowerCore-6750 detects automatically whether it is plugged into slot 1 and if the switches SW7-1 and SW7-2 are set accordingly (see table 8 “Default Switch Settings” on page 16).
The board may also be programmed to be system controller via Universe II.

Slot-1 (System Controller) Functions

If the CPU board is a slot-1 device, PPC/PowerCore-6750 sets up the required system controller functions:

- Enable the arbiter (see section “Requester” on page 66)
- Drive SYSCLK to the VMEbus (see “SYSCLK Driver” on page 64),
- Drive floating bus grant levels 0, 1, 2, and 3

- Allow the Universe II bus timer to terminate VME cycles (timeout), if the bus timer is enabled (see section 4.10.7 “VMEbus Timer” on page 65)

Slot-1 Auto-detection

The board’s slot-1 auto-detection mechanism probes the VMEbus bus-grant-in-level-3 pin (BG3IN*) during power up to see whether it is possible to pull this signal down to a low-signal level.

- When PPC/PowerCore-6750 is plugged into slot 1, it will succeed in pulling the VME signal to a low-signal level, because BG3IN* is floating on slot 1. Hence, the CPU board detects slot 1.
- When PPC/PowerCore-6750 is not plugged into slot 1, it will receive the BG3IN* from a board plugged into a lower slot. It will fail trying to pull the VME signal to a low-signal level. Hence, the CPU board detects not being plugged into slot 1.

Manual Slot-1

The following situation may cause PPC/PowerCore-6750 to detect being plugged into slot-1 although actually being plugged into a different slot:

> A VMEbus system begins with the highest daisy-chain priority at slot 1, the left most slot. The higher the slot number, the lower the daisy-chain priority. As the slots move right they lose daisy-chain priority, so slot 2 has higher daisy-chain priority than slot 3, and slot 3 has higher daisy-chain priority than slot 4, and so on. When a board which is not compliant with ANSI-VITA 1-1994 is plugged into a slot with higher daisy-chain priority, auto-detection may fail. This occurs if the higher daisy-chain priority board does not drive the bus-grant-out-level-3 (BG3OUT*) on the VMEbus to the high-signal level as defined by ANSI-VITA 1-1994.

In this situation PPC/PowerCore-6750 probes its BG3IN* at a low-signal level and concludes that slot 1 is detected. However, the conclusion does not fit the actual system setup. To prevent any mismatch you can enable or disable the slot-1 function manually:

1. Disable the auto-detection by setting SW7-1 appropriately: ON = autodetection disabled (default “OFF”, see page 17)
2. Enable or disable the slot-1 functions manually by setting SW7-2 appropriately: ON = slot-1 function enabled (default “OFF”, see page 17).

Slot-1 Status

The Universe II register MISC_CTL can be used to read the status of the slot-1 configuration.

SYSCLK Driver

The CPU board contains all necessary circuits to support the SYSCLK signal. The output signal is a stable 16-MHz signal. The driver circuitry for the SYSCLK signal can source a current of 32 mA at high level and sink a current of 64 mA at low level.

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The SYSCLK signal will be enabled if:

- Slot 1 has been detected by auto-detection
- Slot 1 has been detected due to the switch setting
- Set by software (see section 6.8 “VMESYS – Enabling VMEbus System Controller” on page 103)

SYSCLK will be driven until the CPU board is powered down or low voltage is detected at the low-voltage monitor.

4.10.7 VMEbus Timer

Universe II provides:

- VMEbus timer to terminate VME transfers by generating a bus error when no acknowledge is detected after a programmable timeout period
- VMEbus arbiter timer which can be enabled only when the CPU board provides system controller functions. The timeout periods can be configured in the Universe II register MISC_CTL

4.10.8 VMEbus Arbitration and VMEbus Requester

Each transfer to or from an off-board address causes a VMEbus access cycle which is carried out in accordance with the arbitration mechanism defined for the VMEbus. PPC/PowerCore-6750 includes:

- VMEbus arbiter so that it may act as slot-1 system controller (see section 4.10.6 “VMEbus Slot-1 Functions” on page 63)
- VMEbus requester so that it may access external VMEbus resources

Arbitration Modes

PPC/PowerCore-6750 includes one of the following arbitration modes programmable via the Universe II MISC_CTL register:

- Four-level fixed-priority arbitration mode
- Single-level arbitration mode
- Four-level round-robin arbitration mode (default)

Note: **According to ANSI-VITA 1-1994, the arbiter must be enabled if the CPU board is located in slot 1 of the VMEbus backplane. The arbiter must be disabled if the CPU board is located in any other slot. Single-level arbitration is a subset of fixed-priority arbitration mode. To achieve single-level arbitration mode, set Universe II to fixed-priority mode. The VMEbus mastership is granted only on level three.**

Requester

PPC/PowerCore-6750 includes a VMEbus requester so that it may access external VMEbus resources.
The request level is programmable via the Universe II MAST_CTL register (see "PCI-to-VME bridge – Universe II", *Data Sheets*).

Note: **The selection of the VMEbus request level does not depend on the VMEbus arbiter located in Universe II.**

Release Modes

PPC/PowerCore-6750 provides several software-selectable VMEbus release modes to release VMEbus mastership. The bus release operation is independent of the fact whether the on-board VMEbus arbiter is enabled and of the VMEbus arbitration level. Easy handling and use of the VMEbus release modes is provided by Universe II programmable in the MAST_CTL register.
Before the bus is released a read-modify-write (RMW) cycle in progress is always completed.

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–ROR
- In the release on request (ROR) mode bus mastership is released when another VMEbus board requests bus mastership while the CPU board is the current bus master. Ownership of the bus may be assumed by another channel (e.g Universe II DMA channel) without rearbitration on the bus if there are no other requests pending.

–RWD
- In the release when done (RWD) mode the VME master interface releases the VMEbus ownership, when the channel accessing the VMEbus has transferred its data.

4.11 Ethernet Interface

PPC/PowerCore-6750 offers a Local Area Network (LAN) interface at the front panel. This LAN interface is based on:

- Ethernet controller located at the PCI bus
- Ethernet interface adapter
- Filter transformer routing the two receive and the two transmit lines of the 10Base-T or 100Base-TX interface to the Ethernet interface adapter.

Ethernet Address

The unique Ethernet address is permanently stored at the ID-ROM. After power-on the Ethernet address is copied into the NVRAM at offset $1C12_{16}$ where it can be read by the software.

Features

The Ethernet interface provides the following features:

- Compatibility with IEEE 802.3/Ethernet
- Data rate of 100 Mbit/s
- DMA capability
- Interrupt generation

4.11.1 Ethernet Controller

The fast Ethernet LAN controller provides the following features:

Integration Features

- Integration features
  - Integrated PCS and scrambler/descrambler for CAT5
  - Integrated AUI port routed to PN15 (factory option) (see figure 2 “PN15 Connector Pinout” on page 22)
  - Autonegotiation of full-duplex and half-duplex operation for 10 and 100 Mbit/s (NWAY)

Performance features

- Performance features
  - Support of PCI read multiple, read line, and write and invalidate commands
  - Direct memory access (DMA) with programmable burst size provided for low CPU utilization
  - Unlimited PCI burst support
  - Support of early interrupt on transmitting and receiving
  - Support of a variety of flexible address filtering modes (including perfect, hash tables, inverse perfect, and promiscuous)

Device Features

- Device features
  - Support of big or little endian byte ordering for buffers and descriptors
  - Support of full-duplex operation on MII port
  - Low-power management with 2 power-saving modes (sleep and snooze)
  - Internal and external loopback capability on all network ports
  - LED support for network activity indications
  - JTAG-compatible test-access port with boundary-scan pins
  - Low-power 3.3-V CMOS technology
  - Maximum supply current after power-up: 70 mA

Automatic Detection and Sensing Features

- Automatic detection and sensing features
  - Support of IEEE 802.3 autonegotiation algorithm of full-duplex and half-duplex operation for 10 and 100 Mb/s

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CSR Base Address — The CSR base address of the Ethernet controller is $\texttt{FE85.0000}_{16}$.

Interrupt — The Ethernet controller uses INTA # for interrupting the CPU (see table 20 “Default PPC/PowerCore-6750 Interrupt Map” on page 39).

Data Sheets — For more information on programming the Ethernet controller, see “Ethernet Controller – LAN 21143”, *Data Sheets*.

4.11.2 Ethernet Interface Adapter

Features — The Ethernet interface adapter integrates:

- Physical layer integrated in one chip
- MII interface
- 10Base-T and 100Base-TX compliant half and full duplex transceiver,
- Extended register set including detailed status monitoring

Data Sheets — For more information on the Ethernet interface adapter, see “Ethernet Interface Adapter – LXT970 and ICS 1890”, *Data Sheets*.

4.12 PCI-to-ISA Bridge

Master/Slave Interfaces — The PCI-to-ISA bridge provides:

- PCI master/slave interface with 33 MHz
- ISA master/slave interface with 8.25 MHz

Timer/Counter — The PCI-to-ISA bridge integrates a timer/counter with three channels.

Interrupt Controller — In addition, the PCI-to-ISA bridge includes two interrupt controllers supporting 15 interrupt channels. These interrupt controllers can be programmed independently of edge or level sensitivity.

DMA Functions — The PCI-to-ISA bridge has two DMA controllers and seven independently programmable channels.

NMI — The PCI-to-ISA bridge integrates a control logic generating non-maskable interrupts (NMIs).

Multifunctional Device — The PCI-to-ISA bridge is a multifunctional device: the bridge is function 0, the IDE controller (not used on this CPU board) is function 1. Both can be configured independently.

Data Sheet

For more information on the PCI-to-ISA bridge and the IDE interfaces, see “PCI-to-ISA Bridge – W83C553F”, *Data Sheets*.

4.12.1 PCI-to-ISA Function

The PCI-to-ISA-bridge prevents the slower I/O devices from slowing down the PCI bus.

Devices on the ISA Bus

The following devices are located on the ISA bus:

- Two serial interfaces
- NVRAM and RTC
- CIO for internal control
- DCCR
- PN15 connector (factory option) for ISA extension

ISA Base Address

The ISA base address of the PCI-to-ISA bridge is $\texttt{FE00.0000}_{16}$.

4.12.2 Interrupt Controller

The following figure shows the default interrupt structure of the CPU board. The interrupt controller of the PCI-to-ISA bridge is used for interrupt routing. The PCI-to-ISA bridge collects the possible interrupts and passes them to the CPU via the INTR line. An NMI is generated only when:

- PCI system error (PCI signal SERR# active) occurs
- Watchdog timeout occurs
- ABORT key is pressed

All interrupts can be disabled independently.

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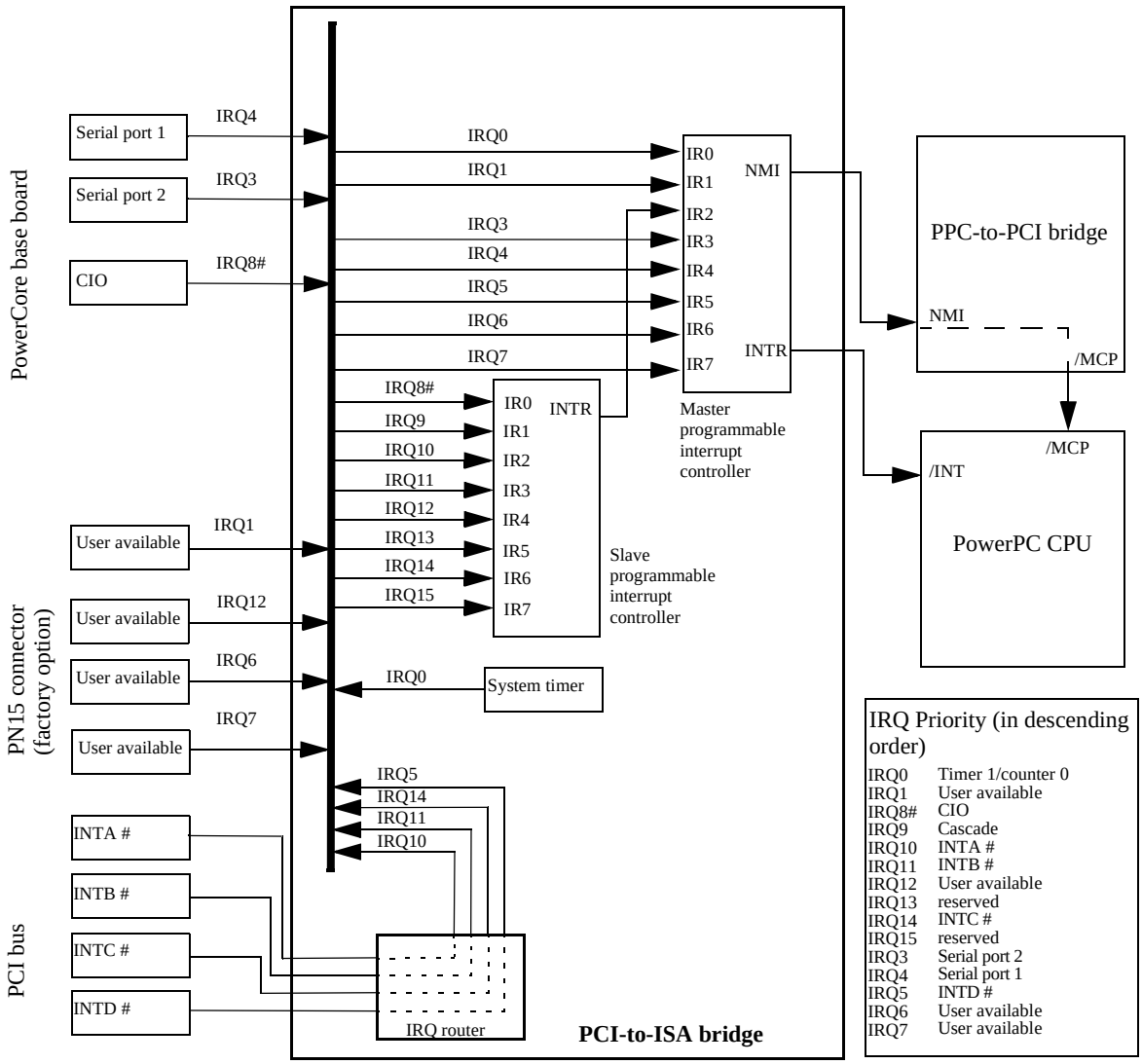
Figure 6 Default PCI-to-ISA Bridge Interrupt Structure



4.13 Real-Time Clock / Non-Volatile RAM

The real-time clock (RTC) and the non-volatile RAM (NVRAM) are housed in one device including a battery backup.

Features of the Battery

The battery is mounted as snaphat on top of the device with a direct connection to its power supply. For information on exchanging the battery, see section 1 “Safety Notes” on page 1 and **section 3 “Installation” on page 9**.
When the power fails, the device is automatically deselected and changes into write-protected mode.

Address Space

The RTC/NVRAM address space is divided into three parts.

Table 39 Address Space of the RTC/NVRAM

Address Range	Access
0000_{16} … $1BFF_{16}$	NVRAM user defined area
$1C00_{16}$ … $1FF0_{16}$	NVRAM configuration area
$1FF1_{16}$ … $1FF7_{16}$	unused
$1FF8_{16}$ … $1FFF_{16}$	RTC registers

Address Access to the RTC/NVRAM

The access to the RTC/NVRAM is 8-bit wide and indirect.
To access a location within the device:

1. Write the lower address byte to address $FE00.0073_{16}$ (write-only),
2. Write the higher address byte to address $FE00.0075_{16}$ (write-only),
3. Read or write data from or to address $FE00.0077_{16}$.

NVRAM

Since the last 16 bytes are used for the RTC or unused, the NVRAM has a capacity of 8 KByte — 16 bytes. The complete address space of the NVRAM is 0000_{16} … $1FF0_{16}$.

User Defined Area

The user may store important data in the user defined area of the NVRAM.

Configuration Area

The NVRAM configuration area is used for internal configuration data.

Note: **The user must not change the values stored in the configuration area.**

Features of the RTC

The on-board RTC maintains accurate time and date based on its own crystal. The on-board RTC is year-2000 compliant.

Data Sheet

For more information on the registers and the operation of the RTC, see “Real-Time Clock and NVRAM – RTC/NVRAM M48T58”, *Data Sheets*.

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4.14 PPC/PowerCore-6750 Parameters and Timers – CIO

The configuration and status information for several PPC/PowerCore-6750 parameters and timers are accessible via an 8-bit register, the CIO data and timer registers, and the NVRAM configuration area. They are all located on the ISA bus.

4.14.1 Parameters

Some of the following parameters can only be read, others can be read and written:

– DRAM	reading the DCCR (see table 24 “DCCR, Bits [5…0]” on page 46)
– Cache	reading the DCCR (see table 22 “DCCR, Bits [7…6]” on page 41)
– Boot flash	writing parameters of the boot flash devices via CIO port A (see table 28 “CIO Port A Data Register, Bits [7] and [4]” on page 50)
– User flash	writing parameters of the user flash devices via CIO port A (see table 32 “CIO Port A Data Register, Bits [7], [3…2], and [0]” on page 54)
– Boot parameters	reading the boot parameters from the NVRAM (see section 4.13 “Real-Time Clock / Non-Volatile RAM” on page 71)
– ID-ROM	the ID-ROM includes different parameters internally used.
– BUSMODE	The PMC BUSMODE signals can be set and read via CIO port B (see table 44 “CIO Port B Data Register, Bits [5…1]” on page 77).

4.14.2 Timers

PPC/PowerCore-6750 includes five different timers:

- The PowerPC CPU provides a 64-bit timer.
- The PCI-to-ISA bridge provides a system timer (counter 0, IRQ 0) (see “PCI-to-ISA Bridge – W83C553F (http://www.winbond.com)”, *Data Sheets*).

The CIO provides three independently programmable 16-bit timers with 500-ns resolution which can also be used as counters (see “CIO Counter/Timer – CIO Z8536”, *Data Sheets*).

The peripheral clock of the CIO device is connected to a 4.125-MHz source.

4.14.3 CIO

PPC/PowerCore-6750 integrates one CIO which controls internal signals and devices. The CIO includes the 3 independently programmable ports A, B, and C.

Features of the CIO

The CIO contains:

- Two independent 8-bit ports (ports A and B)
- One special-purpose 4-bit port (port C)
- Three independently programmable 16-bit timers which can also be used as counters

Base Address

$FE00.0300_{16}$

IRQ

The interrupt request output of the CIO uses IRQ8#.

Data Sheet

For information on programming the timers and the ports, see “CIO Counter/Timer – CIO Z8536”, *Data Sheets*.

4.14.4 CIO Port A Data Register

Table 40 CIO port A Data Register

FE00.0302								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	VPP_CTRL	ISA_IDENT	reserved	BOOT_A20	FLSH_SEL[1…0]		reserved	USER_A20

VPP_CTRL

see table 28 “CIO Port A Data Register, Bits [7] and [4]” on page 50 or table 32 “CIO Port A Data Register, Bits [7], [3…2], and [0]” on page 54

ISA_IDENT (R)

see table 45 “CIO Port A Data Register, Bit [6]” on page 79

BOOT_A20

see table 28 “CIO Port A Data Register, Bits [7] and [4]” on page 50

FLSH_SEL[1…0]

see table 32 “CIO Port A Data Register, Bits [7], [3…2], and [0]” on page 54

USER_A20

see table 32 “CIO Port A Data Register, Bits [7], [3…2], and [0]” on page 54

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4.14.5 CIO Port B Data Register

Table 41 CIO Port B Data Register, Bits [7…6]

FE00.0301$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ID_SCL	ID_SDA	BUSMODE[4…2]			BUSMODE[1…0]		reserved

ID_SCL (W) — ID_SCL controls the ID-ROM SCL signal (I^2C bus).

ID_SDA (R/W) — ID_SDA controls and indicates the status of the ID-ROM serial data signal (I^2C bus).

BUSMODE [4…2] — see table 44 “CIO Port B Data Register, Bits [5…1]” on page 77

BUSMODE [1…0] — see table 44 “CIO Port B Data Register, Bits [5…1]” on page 77

4.14.6 CIO Port C Data Register

Table 42 CIO Port C Data Register

FE00.0300$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	used as masking bits for write accesses to bit 3…0 (e.g.: if bit 4 is 1, bit 0 cannot be written)				WDNMI	TRWD	LED[1…0]	

WDNMI — see table 23 “CIO Port C Data Register, Bit [3…2]” on page 42

TRWD — see table 23 “CIO Port C Data Register, Bit [3…2]” on page 42

LED [1…0] (R/W) — LED [1…0] controls the user LED U at the front panel.

- = 00_2 user LED U is off.
- = 01_2 green user LED U
- = 10_2 red user LED U
- = 11_2 user LED U is off (default)

4.15 Serial I/O Ports – SCCs

PPC/PowerCore-6750 provides two serial I/O ports implemented by two serial communication controllers (SCCs).

Features

The SCCs:

- Run with all existing 16C450 software
- Provide:
  - Programmable baudrate generator
  - Standard asynchronous communication bits
  - Fully programmable serial interface characteristics

Clock Input

The peripheral clock input of the SCCs is driven by a 1.8432-MHz clock.

IRQs

The interrupt requests of the SCCs are connected to the IRQ4 and IRQ3 input of the PCI-to-ISA-bridge.

Table 43 SCC Base Addresses

Serial I/O Port	SCC Base Address
1	$FE00.03F8_{16}$
2	$FE00.02F8_{16}$

RS-232 Interfaces

The serial I/O interfaces are implemented as RS-232 interfaces. They are available at the front panel.

Serial I/O Configuration

For more information on the configuration of the serial ports, see “Serial I/O Port – TL16C550C”, *Data Sheets*.

Connector Pinout

For information on the connectors at the front panel and the connectors’ pinout, see section 3.6 “Serial I/O Ports” on page 20.

Data Sheet

For more information on the SCC, see “Serial I/O Port – TL16C550C”, *Data Sheets*.

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4.16 PMC Slots

PPC/PowerCore-6750 provides two PMC slots.

Power and Requirements

For detailed information on the power and the requirements of the PMC modules, see section 3.1 “Installation Prerequisites and Requirements” on page 10 and section 3.7 “PMC Slots” on page 21.

4.16.1 Busmode

Via the signals BUSMODE [4…0] the host gets information on:

- Presence of PMC modules (= card)
- Logical protocol of the PMC modules

Via the BUSMODE [4…2] signals, which are driven by the host, the PMC modules get the information whether a host is present. The answer of the PMC modules is transferred by the signal lines BUSMODE [1…0]. All signals are compliant with IEEE P1386/Draft 2.0.

Note: **The BUSMODE [4…2] signals must be set accordingly. If port B is not initialized, the PMC modules do not detect the host and do not work. Per default, the firmware initializes the BUSMODE [4…2]signals.**

Table 44 CIO Port B Data Register, Bits [5…1]

FE00.0301$_{16}$								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	ID_SCL	ID_SDA	BUSMODE[4…2]			BUSMODE[1…0]		reserved

ID_SCL	see table 41 “CIO Port B Data Register, Bits [7…6]” on page 75
ID_SDA	see table 41 “CIO Port B Data Register, Bits [7…6]” on page 75
BUSMODE [4…2] (R/W)	BUSMODE[4…2]indicate the meaning of the 3 output signals BUSMODE [4…2] routed to both PMC slots.
= 000_2	Card Present Test: The cards at PMC slot 1 and 2 return "Card Present", if they are plugged into the slot and no bus protocol is used.
= 001_2	Card Present Test: The cards at PMC slot 1 and 2 return "Card Present" if they are PCI capable and PCI protocol is used.
= 010_2	Card Present Test: The cards at PMC slot 1 and 2 return "Card Present" if they are PCI capable and SBus protocol is used.
= 011_2	reserved
= 100_2	reserved
= 101_2	reserved
= 110_2	reserved
= 111_2	no host present
BUSMODE [1…0] (R)	The PMC cards indicate their presence to the given protocol (e.g. PCI protocol, SBus protocol) by the message "Card present". BUSMODE [1] is connected with PMC slot 2, BUSMODE [0] with PMC slot 1.
= 0	card present
= 1	no card present

4.17 ISA Devices

The connector PN15, which is a factory option, may be used to install ISA devices.

Table 45 CIO Port A Data Register, Bit [6]

FE00.0302								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	VPP_CTRL	ISA_IDENT	reserved	BOOT_A20	FLSH_SEL[1…0]		reserved	USER_A20

VPP_CTRL (R/W) — see table 28 “CIO Port A Data Register, Bits [7] and [4]” on page 50 or table 32 “CIO Port A Data Register, Bits [7], [3…2], and [0]” on page 54

ISA_IDENT (R) — ISA_IDENT indicates whether ISA devices are installed at the PN15 connector which is a factory option (see figure 2 “PN15 Connector Pinout” on page 22).

= 0 ISA devices installed.

= 1 no ISA devices installed.

BOOT_A20 (R/W) — see table 28 “CIO Port A Data Register, Bits [7] and [4]” on page 50

FLSH_SEL [1…0] (R/W) — see table 32 “CIO Port A Data Register, Bits [7], [3…2], and [0]” on page 54

USER_A20 (R/W) — see table 32 “CIO Port A Data Register, Bits [7], [3…2], and [0]” on page 54

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Please Note…

The *PowerBoot Instruction Set* is an integral part of the *PPC/PowerCore-6750 Reference Guide* (P/N 205021), which is packaged separately.

The *PowerBoot Instruction Set* will always be shipped together with the *Reference Guide*.

Please:

☞ **Insert the *PowerBoot Instruction Set* (P/N 204525) now into the *PPC/PowerCore-6750 Reference Guide* (P/N 205021).**

☞ **Remove this sheet.**

5 PowerBoot (= PowerBoot Instruction Set)

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6 PowerBoot for PPC/PowerCore-6750

This chapter describes the board specific commands of PowerBoot.

Command Overview

PowerBoot includes the following board specific commands:

- Command to manually map the PCI bus devices at PMC slot 1 or 2:

  "PMCPCI – Mapping PMC Modules" on page 87

- Command to restart the CPU board:

  "RESET – Restarting the Board" on page 89

- Command to set and display auto boot after power-on:

  "SETBOOT – Editing Auto Boot Parameters" on page 90

- Command to turn the user LED at the front panel ON or OFF:

  "USERLED – Setting User LED" on page 100

- Command to enable or disable the VMEbus system controller or to indicate its current status:

  "VMESYS – Enabling VMEbus System Controller" on page 103.

- Commands to initialize an A32/D32 master or slave interface to the VMEbus:

  "VMEMST – Opening an A32/D32 Master Window" on page 100
  "VMESLV – Opening an A32/D32 Slave Window" on page 102

NETLOAD and NETSAVE

The two commands `NETLOAD` and `NETSAVE` are independent of the CPU board. Therefore, they are described in the *PowerBoot Instruction Set*. However, they include also an additional board specific option to select the MII or AUI interface. This board specific option is described in section 6.9 "NETLOAD and NETSAVE – Board Specific Option" on page 104.

Supports and Requirements

PowerBoot supports up to 9-MByte on-board flash memory:

- 1-MByte boot flash for PowerBoot, OpenFirmware, or other operating systems, which can always be accessed
- 8-MByte user flash which can be accessed in 8 windows each consisting of 1 MByte

The PowerBoot flash memory must be located at the CPU address $\texttt{FFF0.0000}_{16}$, because the PPC/PowerCore-6750 CPU vectors to the address $\texttt{FFF0.0100}_{16}$ after an active /RESET. Additionally, this flash memory has to be visible to the CPU at all times (no bank switching).

6.1 PPC/PowerCore-6750 Address Map

The following table lists the default addresses of the PPC/PowerCore-6750 board mapped by PowerBoot.

Table 46 PPC/PowerCore-6750 Address Map seen from the CPU

Address	Device	
0000.0000_{16} … $3FFF.FFFF_{16}$	EDO DRAM or SDRAM:	Memory module(s)
4000.0000_{16} … $7FFF.FFFF_{16}$	PPC-to-PCI bridge	
8000.0000_{16} … $FDFF.FFFF_{16}$	PCI memory:	VME windows
$FE00.0000_{16}$	PCI-to-ISA bridge:	Base address of ISA registers
$FE00.0073_{16}$	ISA RTC/NVRAM:	Low-address byte port
$FE00.0075_{16}$		High-address byte port
$FE00.0077_{16}$		Data byte port
$FE00.0300_{16}$ … $FE00.0303_{16}$	CIO parallel port addresses	
$FE00.0308_{16}$	DCCR	
$FE00.0310_{16}$	Chip select signal (PN15 connector: factory option)	
$FE00.03F8_{16}$ … $FE00.03FF_{16}$	Serial console:	I/O port
$FE85.0000_{16}$	Ethernet controller:	Base address of CSR registers
$FE81.0000_{16}$	Universe II:	Base address of CSR registers
$FEC0.0000_{16}$	PCI bus:	Configuration address register (CAR)
$FEE0.0000_{16}$		Configuration data register (CDR)
$FEF0.0000_{16}$	Interrupt acknowledge cycle	
$FFE0.0000_{16}$ … $FFEF.FFFF_{16}$	User flash:	Window for devices 1, 2, 3, 4
$FFF0.0000_{16}$ … $FFF7.FFFF_{16}$	Boot flash (default: 512 KByte):	Device 1
$FFF0.0000_{16}$ … $FFFF.FFFF_{16}$	Boot flash (fact. opt.: 1 MByte):	Device 1

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6.2 PMCPCI – Mapping PMC Modules

PMCPCI manually maps a user mounted PMC module to any location in the PCI addressing space by defining its PCI I/O space address and/or its PCI memory space address. The PCI addressing space is divided into two areas:

Table 47 PCI Addressing Spaces

PCI Addressing Space	Address	PCI Addressing Space Seen from
PCI I/O space	$FE80.0000_{16}$ …$FEBF.FFFF_{16}$	CPU
	0080.0000_{16} …$00BF.FFFF_{16}$	PCI bus master
PCI memory space	8000.0000_{16} …$FCFF.FFFF_{16}$	CPU or PCI bus master

At PPC/PowerCore-6750 the addresses for the local Ethernet devices and the Universe II VMEbus interface are already mapped to the PCI I/O space (see table 46 “PPC/PowerCore-6750 Address Map seen from the CPU” on page 86).

Syntax

PMCPCI *PmcModule PciIOSpaceAddr PciMemSpaceAddr*

PmcModule
defines the PMC module to be mapped:

– 1 = PMC module 1

– 2 = PMC module 2

PciIOSpaceAddr
defines the PCI I/O space address seen from the PCI bus. If the PCI I/O space address is set to 0000.0000_{16}, it will be ignored.

PciMemSpaceAddr
defines the PCI memory space address seen from the PCI bus. If the PCI memory space address is set to 0000.0000_{16}, it will be ignored.

Description

PMCPCI checks the capabilities of every device.

- If the PCI device mounted on a PMC module supports both addressing spaces, the PCI bus device register at offset 10_{16} is used for the PCI I/O space and the PCI bus device register at offset 14_{16} is used for the PCI memory space. In this case both addresses given by the user are programmed in the PCI bus device.

- If a PCI bus device mounted on a PMC module does not support both addressing spaces, only the supported one will be used even if both addressing spaces have been defined.
- If a PCI bus device mounted on a PMC module is able to support both addressing spaces, but only one should be used, set the address which should not be used to $FFFF.FFFF_{16}$.
- If no PCI bus device is installed, one of the following messages appears:

```
PMC 1/2 modules:
Error: Can’t set base-address of PMC1

PMC 1/2 modules:
Error: Can’t set base-address of PMC2
```

Example

In the following example a PMC module at PMC slot 1 is mapped to the PCI memory space 0082.0000_{16} and to the PCI bus memory space 8000.0000_{16}. A user application can access the PCI bus device CSR registers via the PowerPC CPU at the PCI I/O space address $FE82.0000_{16}$ and at the PCI memory space address 8000.0000_{16}.

```
PowerBoot>
PowerBoot>
PowerBoot> PMCPCI 1 00820000 80000000

PMC1/2 modules:
PMC1, PCI address 0x00820000, Base Reg. 0x10, PCI I/O space, Master enable
PMC1, PCI address 0x80000000, Base Reg. 0x10, PCI MEM space, Master enable
Device ID = 0x0009; Vendor ID = 0x1011;
Status    = 0x0280; Command   = 0x0007;
Base Class= 0x02;   Sub Class = 0x00;   Prg. Inter= 0x00;   Rev. ID   = 0x20;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x00;   Cache Line= 0x00;
base addr0= 0x00820001, base addr1= 0x80000000;
Max Lat   = 0x28;   Min Gnt   = 0x14;   IRQ Pin   = 0x01;   IRQ Line  = 0xFF;
Found PCI device: DEC Chip 21140A Fast Ethernet LAN


PowerBoot>_
```

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6.3 RESET – Restarting the Board

The restarting of the CPU board via RESET is not as strong as a power-on reset. RESET incites only a jump to the /HRESET exception vector at $FFF0.0100_{16}$.

Syntax

```
RESET
```

Description

All devices based on the PCI bus will keep their PCI configuration space header region, e.g. the Ethernet controller will keep its default base address. But the EDO DRAM or SDRAM, the PCI-to-ISA bridge, the serial console, the CIO parallel port, the Ethernet controller, the VMEbus interface etc. will be initialized. The L1 cache and L2 cache will be flushed and invalidated.

Example

```
PowerBoot> RESET
Init serial 1 at address: 0xFE0003F8
Init serial 2 at address: 0xFE0002F8
Init CIO at address: 0xFE000300
Init Ethernet Controller at address: 0xFE850000
Init UNIVERSE VMEbus device at address: 0xFE810000
PowerCore is -NOT- VMEbus System Controller (SYSCON=0)
Testing NVRAM.....................done
Testing RAM ......................done
Testing Boot FLASH....CSUM 0x20A7..done
Testing PCI Bus ..................done
Testing ISA ......................done
Testing Ethernet Controller........done
Found CPU740/750, PVR=00088201,
CPU clock: 233MHz, Bus clock: 66MHz
DRAM EDO mode enabled, DRAM ECC mode enabled
Onboard DRAM      : none
Init DRAM Module 1:  16MB, 0x00000000..0x00FFFFFF
Init DRAM Module 2:  none
Init DTLB/ITLB for block translation, enable MMU
Init L1-Icache
Init L1-Dcache
Init L2-Cache, found 1024 kByte cache, 146MHz
Init exception vectors starting at address: 0x00000100
Read NVRAM...identify board

<<PowerBoot V2.03 for PowerCore CPU-6750 VME>>

PowerBoot>
```

6.4 SETBOOT – Editing Auto Boot Parameters

SETBOOT prompts the user to enter values for the parameters required for the auto booting. The defined parameters become valid after the next power-on or when RESET is entered. The parameters are stored in the on-board NVRAM which keeps its contents during power-off and checks them after power-on or after RESET has been entered.

Syntax SETBOOT

Description After SETBOOT has been entered, the user is prompted to assign a value to each parameter described in the following. The prompt describes briefly the possible values of the respective parameters and the current setting.

The parameters described in the following

- Define the location of the automatically loaded binary image: `boot select`
- Determine the kind of booting and the location where the binary image is started: `auto boot`, `boot address`, `load address`
- Select a delay for the auto booting after power-on: `auto boot delay`
- Define a byte-sized value which has to be read by the PowerPC CPU and which determines when instructions are executed: `magic wait number`
- Select one of the user flash devices: `boot user_flash`
- Select a harddisk SCSI ID for booting a boot file: `boot disk SCSI ID`
- Select a controller SCSI ID for a mounted PMC module: `PMCx controller SCSI ID`
- Select a boot delay time for waiting after power-on: `boot delay for SCSI disk`
- Select the location and the size of the VMEbus slave window and the location of the VMEbus master window: `VMEbus slave window base` and `size, PCI bus master window base`
- Define the name and the path of the file loaded during auto boot: `TFTP/disk boot file name`
- Select the port to be used with the Ethernet interface: MII on the front panel or AUI via the VMEbus connector P2 and PPC/SSIO-6750: `MII or AUI interface`
- Select the internet protocol for connecting a server to the CPU board: `RARP or ARP protocol`

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- Select the protocol numbers for selecting the TFTP file server and for identifying the CPU board: `serverIP#`, `targetIP#`
- Define the I/O or MEM address seen from the PCI bus which will be written to the PCI bus device of the PMC1 or the PMC2 module: `PMC1 PCI bus I/O base address` and `MEM base address`, same for PMC2

`boot select`
defines the location of the automatically loaded binary image:

– `0` = autoloads a binary image to `boot address` via Ethernet (TFTP and front-panel connector). The user must link the download application image to `boot address`.

– `1` = selects the user flash device preset by `boot user_flash`. Only one user flash device can be mapped to the CPU at address $\texttt{FFE0.0000}_{16}$ (paging). The execution is started at `boot address`.

– `2` = a VMEbus slave interface is opened. The VMEbus slave window is preset by `VMEbus slave window base address` and `size` and by `PCI bus master window base address.` No binary loading nor execution is done. Instead PowerBoot is invoked.

– `3` = a VMEbus slave interface is opened. and a binary image is autoloaded to `boot address` via TFTP. The VMEbus slave window is preset by `VMEbus slave window base address` and `size` and by `PCI bus master window base address`. The execution is started at `boot address`.

– `4` = a VMEbus slave interface is opened and the user flash device defined by `boot user_flash` is assigned to address $\texttt{FFE0.0000}_{16}$. The VMEbus slave window is preset by `VMEbus slave window base address` and `size` and by `PCI bus master window base address.` The execution is started at `boot address`.

– `5` = a VMEbus slave interface is opened. For an outline of the procedure see “magic wait number” on page 92. After the CPU has detected the byte-sized parameter `magic wait number` at the `PCI bus master window base`, a binary image is started at `boot address`. Before `magic wait number` is detected, the wait state can be interrupted for debugging purposes by pressing a key. By this, PowerBoot will be invoked and the binary image is not executed.

– `6` = autoloads a PREP boot image from a SCSI harddisk as described in the PREP specification. If no PREP partition is found, a DOS 4.0 partition will be used. It is assumed that a PMC module is mounted at PMC1 or PMC2, which holds an NCR53C825 or an

NCR53C875 SCSI 2 controller. The user has to prepare the harddisk format to be PREP- compliant or DOS 4.0-compliant. Furthermore, the application image must be prepared for booting. If the partition format DOS 4.0 is used, the pure binary file to be booted can be copied from PC as normal DOS file to the root partition of the harddisk. The parameter `boot address` is used for downloading, `boot disk SCSI ID` for identifying the harddisk, `PMCx controller SCSI ID` is used for identifying the PMC based SCSI controller and `boot delay for SCSI disk` for selecting a delay period after power-on.

`auto boot`
enables or disables the auto booting.

– `0` = auto boot disabled. All NVRAM parameters are ignored. The PowerBoot debugger is invoked.

– `1` = auto boot enabled. Auto boot will take place after the next power-on or when `RESET` is used.

`auto boot delay`
selects a delay ranging from 0 to 99 seconds, i.e. this parameter delays the auto booting by a preset period of time. This is useful for example in case of spinning up a SCSI hard disk drive for booting. During count down of `auto boot delay` the auto booting can be stopped by pressing any user key on the serial console line.

`load address`
specifies the location in the CPU addressing space where the opcode is downloaded. `load address` does not depend on other NVRAM parameters. The binary image is always downloaded to `load address` by using the `boot select` parameters `0`, `3`, `6`.

`boot address`
specifies the location in the CPU addressing space where the opcode is started. It is independent of other NVRAM parameters. The binary image always starts at `boot address,` regardless, whether it is downloaded during power-on or stored in the user flash. For further information on the address map see section 6.1 “PPC/PowerCore-6750 Address Map” on page 86.

`magic wait number`
selects a byte-sized value which appears at `PCI bus master window base address`. It is only used if `boot select` is set to `5`.

The magic wait number enables easy downloading of a user application from a central master CPU to PPC/PowerCore-6750, the target CPU, via the VMEbus backplane. After the master CPU has booted its operating system, it reads every VMEbus location where it expects a

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VMEbus slave window of the target CPU. When a target VMEbus slave window has been found, the master CPU fills every target VMEbus slave window with application code or data. After the transfer has been finished, the master CPU writes the byte-sized value `magic wait number` to every `target VMEbus slave window base`. Every target will read this value and start executing the application instructions at `boot address`.

Opposed to the preceding description, the following paragraph describes the same procedure from the target CPU's perspective.

After power-on, a VMEbus slave window is opened which is defined by `VMEbus slave window base address`, `VMEbus slave window size`, and `PCI bus master window base address`. After this the PowerPC CPU writes its own predefined parameter `VMEbus slave window base address` as long-sized value to `PCI bus master window base address` to indicate to an external VMEbus CPU that PPC/PowerCore-6750 has opened its VMEbus slave window. Then the PowerPC CPU polls the address stored at `PCI bus master window base address`. The PPC/PowerCore-6750 CPU tries to read this address, until the value defined by `magic wait number` is read. This value must be written by another CPU board on the VMEbus to `VMEbus slave window base address`. After the PowerPC CPU has read the `magic wait number`, it starts executing instructions at `boot address`. `Boot address` can be a location at `PCI bus master window base address` or any other location at the CPU addressing space.

`boot user_flash`

selects one of the four 8-bit wide organised user flash devices. The onboard logic of the PPC-to-PCI bridge provides only a 1-MByte sized window at the addressing space for user flash devices. This window ranges from $\texttt{FFE0.0000}_{16}$ to $\texttt{FFEF.FFFF}_{16}$ seen from the CPU addressing space. `boot user_flash` is used only

– if `boot select` is set to `1` or `4`

– and if `auto boot` is set to `1`.

In all other cases `boot user_flash` will be ignored and user flash 1 will always be preset after power-on.

`boot disk SCSI ID`

selects the harddisk SCSI ID for booting the harddisk. `boot disk SCSI ID` is set

– to `0` for harddisk drive 0,

– to `1` for harddisk drive 1,

– to 2 for harddisk drive 2, and so on.

boot disk SCSI ID can range between 0 and 15 and supports wide SCSI drives. boot disk SCSI ID is used only for the auto-boot functionality. Other drives and their SCSI IDs may also be connected but they will be ignored during autobooting. SCSI parity checking is not supported.

PMCx controller SCSI ID
selects the SCSI controller ID for booting the harddisk. PMCx controller SCSI ID is set

– to 0 for SCSI ID 0,

– to 1 for SCSI ID 1,

– to 2 for SCSI ID 2 and so on.

PMCx controller SCSI ID can range between 0 and 15 and supports wide SCSI drives. PMCx controller SCSI ID is used only for the autoboot functionality. It may be changed on demand by an application software. SCSI parity checking is not supported.

boot delay for SCSI disk
selects a delay time ranging from 0 to 99 seconds. boot delay for SCSI disk delays the first access to the harddisk by a preset period of time. It is used only if boot select is set to 6. Other power-on booting options do not use this parameter.

VMEbus slave window base
sets the 32-bit sized base address where the VMEbus slave window can be accessed from the VMEbus (if boot select is set to 5, see “magic wait number” on page 92). There is always one A32/D32 MBLT window opened. For further information see “PCI-to-VME bridge – Universe II”, *Data Sheets*.

VMEbus slave window size
selects the size of the VMEbus slave window (if boot select is set to 5, see “magic wait number” on page 92). The minimum size is 64 KByte and the maximum size is 1956 MByte. The maximum size is limited by the PPC/PowerCore-6750 address map and the 32-bit VMEbus addressing space.

PCI bus master window base
sets the 32-bit sized base address of PCI addressing space where accesses from the VMEbus into the VMEbus slave window are translated into the PPC/PowerCore-6750 memory (if boot select is set to 5, see “magic wait number” on page 92). In general a VMEbus slave window always refers to a PCI bus master window. In most common cases PCI bus master window base holds an address pointing to the PPC/PowerCore-6750 DRAM. Usually this address ranges from

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0000.0000_{16} to the end of the DRAM, i. e. $00FF.FFFF_{16}$ at 16-MByte on-board DRAM.

Note: **The DRAM address range 0000.0000_{16} ... 0001.0000_{16} is used for CPU exception vectors and PowerBoot internals. For further information on the VMEbus interface, see "PCI-to-VME bridge – Universe II",** ***Data Sheets*****.**

PowerBoot checks PMC1 and PMC2 for a mounted PMC module containing one of the following SCSI controllers:

– NCR53C825

– NCR 53C875

If one of the SCSI controllers mentioned above is found, it will be mapped automatically by firmware to the addresses shown in the following table.

Table 48 PCI I/O Addressing Spaces of the SCSI Controllers

PCI I/O Addressing Space	NCR53C825	NCR53C875
Seen from the CPU	$FE82.0000_{16}$	$FE83.0000_{16}$
Seen from the PCI bus	0082.0000_{16}	0083.0000_{16}

Other SCSI controllers are not supported and therefore they will be ignored.

`MII or AUI interface`
specifies the port to be used with the Ethernet interface which will be used for downloading and executing a binary image from a remote system.

– `1` = selects the MII port available on the front panel.

– `2` = selects the AUI port available via the VMEbus P2 connector and a PPC/SSIO-6750.

If another value is entered, the default setting `1` is assigned to the parameter.

`RARP or ARP protocol`
selects the internet protocol used for connecting a server to the CPU board.

– `1` = selects RARP (Reverse Address Resolution Protocol). In case of RARP the parameters `serverIP#` and `targetIP#` are ignored.

– `2` = selects ARP (Address Resolution Protocol). In case of ARP the values entered for the parameters `serverIP#` and `targetIP#` are valid.

If another value is entered, the default setting `1` is assigned to the parameter.

`serverIP#`
defines the internet protocol number which selects the TFTP file server. If the internet protocol RARP is selected, `serverIP#` is ignored. `serverIP#` is stored as string, therefore it has to be written as shown in the following example *123.3.255.255*.

`targetIP#`
defines the internet protocol number identifying the CPU board at internet layer. If the internet protocol RARP is selected, *`targetIP#`* is ignored. *`targetIP#`* is stored as string, therefore it has to be written as shown in the following example *3.255.37.67*.

`TFTP/disk boot file name`
defines the name and path of the file which will be loaded during auto boot (if `boot select` = `0`, `3`, or `6`). The file name including path is at most 128 characters.

If TFTP is used for booting, the host must be set up as TFTP server (`boot select` = `0` or `3`). The host has to be able to provide the desired file via Ethernet (TFTP and front-panel connector).

If a harddisk is used for booting (`boot select` = `6`), it must be set to the corresponding parameters defined by `boot disk SCSI ID`, `PMCx controller SCSI ID`, and `boot delay for SCSI disk`. At first the harddisk partitions 0 to 3 are scanned in order to find a PREP partition (41_{16}). If no PREP partition is found, a DOS 4.0-compatible harddisk partition (06_{16}) will be searched. In case of a valid DOS 4.0 partition, `TFTP/disk boot file name` must be limited to a maximum of 8 characters followed by a dot `.` and an extension consisting of 3 characters (e.g. myfile.bin). All other names are ignored. Do not type a harddisk character like `C:\` in front of `TFTP/disk boot file name`. The root directory of the harddisk partition is searched only for `TFTP/disk boot file name`. Subdirectory levels are not searched and FAT32 systems are not supported.

In both cases (TFTP and harddisk) the user is fully responsible for upper case letters, lower case letters, and the file name itself.

`PMC`*`x`* `PCI bus` *`I/O or MEM`* `base address`
defines the respective I/O or MEM address based on the PCI bus device of the PMC*x* module.

The following description is divided into two parts:

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– First part is a general description of the PMC modules and their base addresses

– Second part describes the four parameters.

On PPC/PowerCore-6750 up to two PMC modules can be installed. Every PMC module can have two different base addresses:

– One base address in the PCI bus I/O space

– One base address in the PCI bus MEM space.

Depending on the features of the installed PMC modules, the addresses have to be set differently:

– If no PMC module is installed, set both addresses to `0`.

– If the installed PMC modules support only one addressing space, set the address which is not supported to $\texttt{FFFF.FFFF}_{16}$ to disable it.

– If the installed PMC modules support both addressing spaces, set both addresses to the desired value.

Note: **Do not set a PMC module base address to an address already used by the on-board PCI bus devices (see table 46 “PPC/PowerCore-6750 Address Map seen from the CPU” on page 86).**

In the following the four parameters are described:

– `PMC1 PCI bus I/O base address`

– `PMC1 PCI bus MEM base address`

– `PMC2 PCI bus I/O base address`

– `PMC2 PCI bus MEM base address`

When defining the I/O base address of PMC*x*, the following is done:

– The PCI bus master bit (bit 2) is set to `1`.

– The PCI bus I/O space control bit (bit 0) is set to `1`.

– The value of the I/O base address is written to offset $\texttt{10}_{16}$, which defines the first I/O base address register in the PCI device header type region.

When defining the MEM base address of PMC*x*, the following is done:

– The PCI bus master bit (bit 2) is set to `1`.

– The PCI bus MEM space control bit (bit 1) is set to `1`.

– The value of the MEM base address is written to offset 14_{16}, which defines the first MEM base address register in the PCI device header type region.

`Power ON Test POT`
is the command to disable the Power On Test (POT) which is executed at boot-up time.

– `1` = disables the Power On Test.

– `0`= enables the Power On Test (default).

The Power On Test results are stored at NVRAM. The results are stored at NVRAM offset `0x1E04` having the bit layout as seen below:

```
DRAM test okay     bit0 = 1, DRAM test fail     bit0 = 0;
PCI test okay      bit1 = 1, PCI test fail      bit1 = 0;
ISA test okay      bit2 = 1, ISA test fail      bit2 = 0;
BootFlash CRC okay bit3 = 1, BootFlash CRC fail bit3 = 0;
Ethernet okay      bit4 = 1, Ethernet fail      bit4 = 0;
NVRAM test okay    bit5 = 1, NVRAM test fail    bit5 = 0;
```

Therefore a fully functional PPC/PowerCore-6750 will show the value `0x3F` for all test okay. A failure will not stop the power-up process of the PPC/PowerCore-6750, because debug functionality must be provided via console serial interface 1. The Power On Test is shown like:

```
Testing NVRAM.....................done
Testing RAM ......................done
Testing Boot FLASH....CSUM 0x20A7..done
Testing PCI Bus ..................done
Testing ISA ......................done
Testing Ethernet Controller........done
```

If the Power On Test is disabled, a value of `0x00` is stored at NVRAM offset `0x1E04` to indicate that no test results are available. It is indicated like:

```
Power On Test disabled
```

After the last parameter has been typed in, a checksum is calculated to protect the NVRAM contents from $1C00_{16}$ to $1FF0_{16}$ containing all edited parameters.

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Example

```
PowerBoot>
PowerBoot> SETBOOT

 -General boot parameters-

Boot select [0=Net, 1=Flash, 2=VME, 3=VME+Net, 4=VME+Flash,
             5=VME+Magic, 6=SCSI disk],  (6) :
Auto boot   [0=disable, 1=enable], (0)   :
Load address (00100000) :
Magic wait number (EA) :
Boot USER_FLASH [1..4], (1) :
Boot Disk SCSI-ID [0..15], (1) :
PMCx Controller SCSI-ID [0..15], (7) :
Boot delay for SCSI Disk [0..99s], (8) :

 -VMEbus boot parameters-

VMEbus slave window base address  (C8000000) :
VMEbus slave window size (00800000) :
PCIbus master window base address (00800000) :

 -TFTP Ethernet/Harddisk boot file parameters-

MII [1] or AUI [2] interface : (1) :
RARP [1] or ARP [2] protocol : (2) :
Server-IP# [aaa.bbb.ccc.ddd] : 192.1.40.21 :
Target-IP# [aaa.bbb.ccc.ddd] : 192.7.405.222 :
TFTP/Disk Boot file name :
pcore603 :

 -PMC modul mapping parameters-

PMC1 PCIbus 0000000) :
PMC1 PCIbus MEM base address (00000000) :
PMC2 PCIbus I/O base address (00000000) :
PMC2 PCIbus MEM base address (00000000) :
CSUM : 0xA5C
PowerBoot>
```

6.5 USERLED – Setting User LED

USERLED defines the color of the user LED at the front panel. The on-board user LED lights red, green, or can be turned off.

Syntax

USERLED *color*

color

defines the color of the user LED:

- *red* = user LED U lights red
- *green* = user LED U lights green
- *dis* = user LED U is off

Example

In the following example the user LED U lights green:

```
PowerBoot> USERLED green
PowerBoot> _
```

6.6 VMEMST – Opening an A32/D32 Master Window

VMEMST initializes an A32/D32 master interface to the VMEbus. The PCI and VME address as well as the window size have to be 64k-aligned. If they are not aligned, an error message is displayed and the slave window is not invoked.

Syntax

VMEMST *PciAddr VmeAddr windowSize reqLevel mode*

PciAddr

specifies the PCI bus address where the VME window is accessed. *pciAddr* has to be located between 8000.0000_{16} and $8FFF.FFFF_{16}$ of the PCI memory.

VmeAddr

specifies the VMEbus address where the master window starts.

windowSize

specifies the size in byte of the VMEbus master window.

reqLevel

specifies the VMEbus request level. The possible values range from 0 to 3:

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– `0` = VMEbus request level 0

– `1` = VMEbus request level 1

– `2` = VMEbus request level 2

– `3` = VMEbus request level 3

`mode`
selects one of the data transfer operations:

– `0` = BLT (Block Transfer)

– `1` = MBLT (Multiplexed Block Transfer)

Description

To initialize a VME master interface, the VME device has to be set up. A VMEbus master interface requires a PCI bus slave interface to be accessed by the CPU. The PCI bus slave interface 0 is used to setup the VME master interface.

If `mode` is set to `0`, the following parameters are selected:

- VMEbus Maximum Data Width (VDW) = 10_2, i.e. 32-bit data width
- VMEbus Address Space (VAS) = 010_2, i.e. A32 addressing space
- Program/Data AM Code (PGM) = 00_2, i.e. data AM code
- Supervisor/User AM Code (SUPER) = 01_2, i.e. privileged mode
- VMEbus Cycle Type (VCT) = 0_2, i.e. single cycle mode

If `mode` is set to `1`, the following parameters are selected:

- VMEbus Maximum Data Width (VDW) = 11_2, i.e. 64-bit data width
- VMEbus Cycle Type (VCT) = 1_2, i.e. single cycle and block transfer mode

The other parameters (VAS, PGM, SUPER) are not changed, i.e. they retain the selections as shown above.

Example

The following example shows a setup of a VME master window of 1 MByte at address 8000.0000_{16}. Every CPU ranging locally from 8000.0000_{16}...8010.0000_{16} accesses the VMEbus between $C800.0000_{16}$ and $C810.0000_{16}$. The VMEbus is requested at level `3` and block transfer is selected.
If the setup has been successful, the following message is displayed:

```
PowerBoot> VMEMST 80000000 c8000000 100000 3 0
Init VME Master Window PCI address:80000000
VME address:                       C8000000
Window size:                       100000
VMEbus request level:               03
VMEbus cycle type (BLT=0, MBLT=1): 0
```

6.7 VMESLV – Opening an A32/D32 Slave Window

VMESLV initializes an A32/D32 slave interface to the VMEbus. The PCI and VME address as well as the window size have to be 64k-aligned. If they are not aligned, an error message is displayed and the slave window is not invoked.

Syntax

VMESLV *PciAddr VmeAddr windowSize*

PciAddr
specifies the PCI bus address where the VME slave window is accessed. It has to be an address of the PCI memory space.

VmeAddr
specifies the VMEbus address where the slave window starts.

windowSize
specifies the size in byte of the VMEbus slave window.

Description

To initialize a VME slave interface the VME device has to be set up. The VMEbus slave interface requires a PCI bus master interface. The PCI bus master interface 0 is used to setup the VME slave interface.

The following parameters are selected:

- VMEbus Address Space (VAS) = 10_2, i.e. A32 addressing space
- Program/Data AM Code (PGM) = 11_2, i.e. both data AM codes
- Supervisor/User AM Code (SUPER) = 00_2, i.e. both user modes

Example

The following example shows a setup of a VME slave window of 1 MByte at address 0040.0000_{16}:

```
PowerBoot>
PowerBoot>
PowerBoot> vmeslv 400000 c8000000 100000
Init VME Slave Window using:
PCI master base address: 00400000
VME slave base address: C8000000
Window size: 00100000

PowerBoot>
```

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6.8 VMESYS – Enabling VMEbus System Controller

VMESYS enables or disables the on-board VMEbus system controller or shows its current status. When enabling or disabling the VMEbus system controller, the setting of SW7-1 and SW7-2 is temporarily overridden.

Syntax

VMESYS *status*

status
defines whether the VMEbus system controller is enabled or disabled:

- ena (or short: e) = VMEbus system controller enabled
- dis (or short: d) = VMEbus system controller disabled
- ? = indicates the current status of the VMEbus system controller

Description

If the VMEbus system controller is enabled, PPC/PowerCore-6750 has to be mounted at slot 1 of the VMEbus backplane. The VMEbus system controller is located in the Universe II PCI bus device. Only the SYSCON bit at register offset 0404_{16} (MISC_CTL) is set or cleared. All other registers keep their settings.

During power-on SW7-1 and SW7-2 are read by the VMEbus interface to enable or disable the VMEbus system controller (see section 3.3 “Switch Settings” on page 15). VMESYS is capable of overriding the switch setting for debugging purposes. An enabled system controller is indicated by a green user LED regardless of the state defined by USERLED (see section 6.5 “USERLED – Setting User LED” on page 100).

Example

To enable the VMEbus system controller enter:

```
PowerBoot> VMESYS ena
PowerBoot> _
```

6.9 NETLOAD and NETSAVE – Board Specific Option

NETLOAD and NETSAVE are independent of the CPU board. Therefore, they are described in the *PowerBoot Instruction Set*. In this section only a board specific option is described.

PPC/PowerCore-6750 provides two Ethernet ports. To define the port to be used with the Ethernet interface, NETLOAD and NETSAVE include an additional option -p.

Syntax

NETLOAD *[-p port] filename address …*

NETSAVE *[-p port] filename address …*

port
specifies the Ethernet port which will be used for downloading binary images from a remote system or saving memory areas into a file. If -p is not specified, the MII port will be selected.

– MII = MII port available on the front panel of the CPU board

– AUI = AUI port available via the VMEbus P2 connector and PPC/SSIO-6750

filename
see *PowerBoot Instruction Set*

address
see *PowerBoot Instruction Set*

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Product Error Report

PRODUCT:	SERIAL NO.:
DATE OF PURCHASE:	ORIGINATOR:
COMPANY:	POINT OF CONTACT:
TEL.:	EXT.:
ADDRESS: _____ _____ _____	
PRESENT DATE:	
AFFECTED PRODUCT: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS	AFFECTED DOCUMENTATION: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS
ERROR DESCRIPTION: _____ _____ _____ _____ _____ _____ _____ _____ _____ _____	

THIS AREA TO BE COMPLETED BY FORCE COMPUTERS:

DATE:

PR#:

RESPONSIBLE DEPT.: ❑ MARKETING ❑ PRODUCTION
ENGINEERING ➠ ❑ BOARD ❑ SYSTEMS

✉ Send this report to the nearest Force Computers headquarter listed on the back of the title page.