PMC551 Hardware Reference and Installation Manual

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Preface

Purpose

This manual describes the design and operational features of the PMC551 PCI DRAM Memory Module as well as installation procedures for attaching the card onto a host Single Board Computer (SBC).

Notice

The information in this manual has been carefully reviewed and is believed to be entirely accurate. However, **RAMiX** shall not be liable nor responsible for errors contained herein.

RAMiX reserves all rights to make any changes to improve the reliability, function or design, without any notice.

Conventions

This manual uses the following conventions:

Convention	Meaning
Return	Press the key that executes commands or terminates a sequence. This key is labeled Return or Enter depending on your keyboard.
<CTRL> X	While you hold down the Ctrl key, press any other key. **RAMiX** monitor commands are case sensitive. You must enter commands in the correct case, as printed in the text.
Courier type	Indicates examples of system output or user input.
Italics	In commands and examples, *italics* indicate a value (e.g., the name of a file) that you should supply.
[ ]	Square brackets in command descriptions enclose the optional command qualifiers. Do not type the brackets when entering information enclosed in the brackets.
|	A vertical bar in command descriptions indicates that you have a choice between two or more entries. Select one entry unless the entries are optional.
{ }	Braces indicate that you are required to specify one (and only one) of the enclosed options. Do not type the braces when you enter the command.
( )	Parentheses enclose a set of options that must be specified together.
0xNNNN	Hexadecimal values are indicated with the 0x prefix.

1 GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes operation, configuration and installation instructions for the **RAMiX,** PMC551 PCI Mezzanine Card (PMC). The PMC551 provides a high performance memory subsystem on the PCI I/O bus. The PMC551 memory will respond with low bus overhead and high determinism. These features can be critical in high performance data acquisition systems.

1.2 FEATURES

The PMC551 complies with the CMC specification for PCI Mezzanine Cards. As such, it will directly connect to any Single Board Computer (SBC), or Expansion Card that supports PMC modules. All initialization and functional configuration of the PMC551 is done automatically by software. Features implemented on the PMC551 include:

- High performance DRAM memory
- All configuration via PCI initialization transactions.
- Can sustain data transfer at full PCI bandwidth.
- No retry on PCI read
- Internal read ahead for zero wait state burst reads

2 HARDWARE INSTALLATION

2.1 Introduction

This chapter provides unpacking, hardware preparation and installation procedures for the PMC551 module.

2.2 Unpacking Instructions

RAMiX boards are protected by an anti-static envelope and/or wrapping. Observe anti-static precautions and work at an approved anti-static workstation when unpacking the board

Note: *The PMC551 is shipped in an individual, reusable shipping box. When you receive the shipping container, inspect it for any evidence of physical damage. If the container is damaged, request that the carrier's agent be present during unpacking and inspection of the unit.*

Unpack the PMC551 module from shipping carton. Check and verify that all items are present by referring to the packing list.

2.2.1 Included Items

Each PMC551 is shipped with the following items:

- PMC551 PMC Assembly

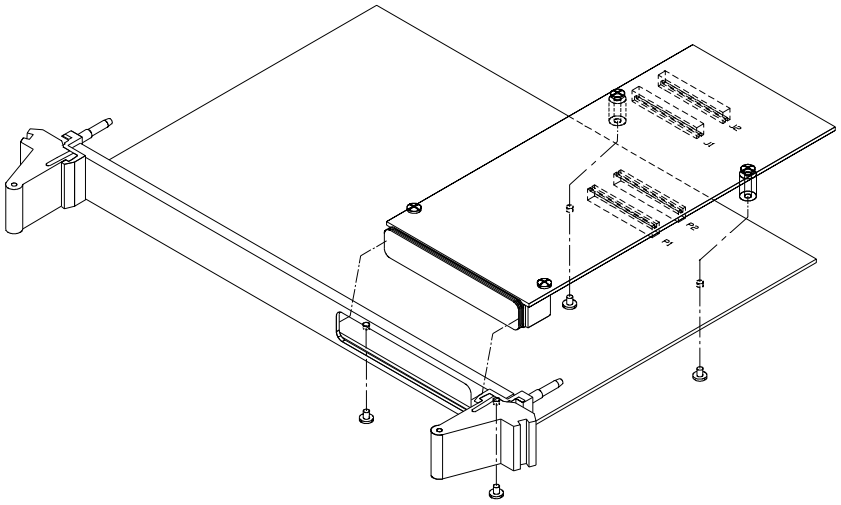
2.3 Handling

Electronic assemblies use devices that are sensitive to static discharge; this applies to both the PMC551 and the host board onto which it will be mounted. Observe anti-static procedures when handling these boards. The PMC551 should be in an anti-static plastic bag or conductive foam for storage or shipment.

2.4 PMC551 INSTALLATION

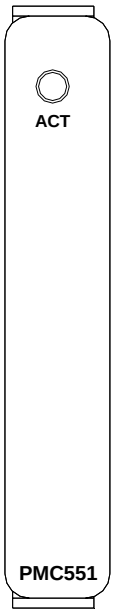
The PMC551 Module is now ready for installation. Turn all system power off. Remove the host board from the chassis (if currently installed). Locate the PMC connectors on the host board. Carefully plug the PMC551 into the mating connectors on the host's printed circuit board. Be sure module is seated properly into CMC connectors on the host. Use screws to fasten module into host PCB.

(See below):



1. Remove the four screws from bottom of the stand-offs of the PMC551
2. Line-up the J1 & J2 on the host PCB to PMC551, J1 & J2
3. Push the PMC551 down (make sure the connectors J1 and J2 are positioned properly).
4. Use the four screws to connect the PMC551 stand offs to the host PCB.

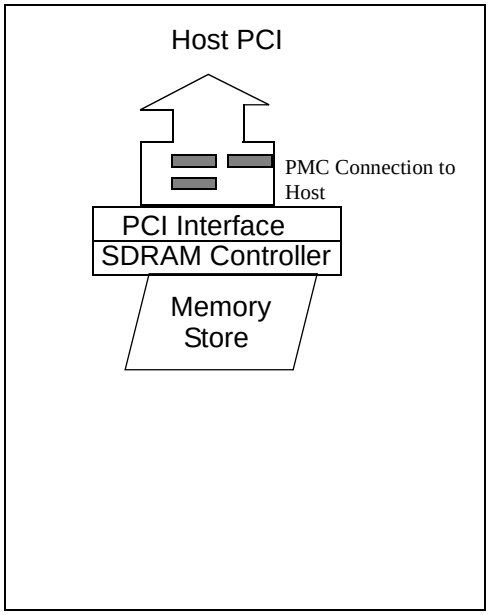
3 Front Panel Indicators



PMC551 Front Panel

4 PMC551 Architecture

The PMC551 is a complete I/O subsystem, illustrated in the block diagram.



4.1 PMC551 Subsystems

The PMC551 features an integrated PCI interface with SDRAM (Synchronous DRAM) memory controller.

4.1.1 Memory Store

Memory configurations range from 32Mbyte to 1Gbyte. All internal configuration information is set during manufacture by RAMiX. A feature of the memory technology used on the PMC551 (SDRAM) requires that the memory be brought to an operational state. This requires performing a sequence of PCI configuration transfers (see the **Programming Notes** section for details).

4.1.2 PCI Interface

The PCI interface on the PMC551 is fully compliant with the PCI 2.1 specification. For data transfer (i.e., access to the memory system), it responds to all PCI READ and WRITE transactions. Configuration and setup is performed using PCI Configuration cycles.

The available memory on a PMC551 can be determined using the standard PCI procedure to query a device for required address space (see the **Programming Notes** section).

Note: (the requested address range will correspond to the amount of memory actually configured on the card, not the maximum possible.)

5 Programming Notes

The PMC551 PCI Interface will respond to PCI configuration cycles upon power-up and PCI Memory cycles, when enabled. The Configuration Space registers include the standard PCI header as well as a number of PMC55 specific registers. (The latter are all in the device-specific address range as provided for in the PCI specification). These latter registers are used after power on to “wake up” the memory. A detailed description of the registers is not provided, as no modification of the sequence is supported.

5.1 Standard PCI Configuration Header

The full set of PCI configuration registers is included in the PCI header, but only a subset are relevant to the operation of the PMC551. As it is only a PCI target, none of the bus master registers will be effective (e.g., Latency Timer). In the following tables registers are presented as 32 bit values; in some cases this is a combination of several smaller registers. This approach is taken for simplicity, access in smaller (i.e., 8 or 16 bit) transfers is supported as documented in the PCI 2.1 specification.

Offset	Description	Default Value
0x0	Device/Vendor ID	0x100011B0
0x4	Command Status Register	0x00000000
0x8	Revision/Class	0x05800000
0xC	Unused on PMC551	0x00000000
0x10	BAR0 (PCI Base Address)	0x00000000
0x14	BAR1 (Unused)	0x00000000
0x18	BAR2 (Unused)	
0x1C	BAR3 (Unused)	
0x20	Reserved	
0x24	Reserved	
0x28	Reserved	
0x2C	SubVendor Device/ SubVendor ID	0x0551140B

5.1.1 Command Status Register

This register is used to enable memory response of the PMC551 and report

Bit(s)	Function
0	Not implemented
1	Memory Enable - When set allows PMC551 to respond to PCI transfers. Must be set after programming BAR0 to allow access to the FailOver firmware
2..5	Reserved
6	Parity Enable. Set to 1 to report cause PMC551 to report parity errors
7	Reserved
8	System Error Enable. When 1 the PMC551 will also assert SYSERR when reporting a parity error
9..22	Unused
23	Fast Back to Back. PMC551 will always correctly respond to fast back to back cycles
24	0
25..26	Device Select timing. Read Only

27..29	Reserved
30	System Error. Set to 1 in response to system error detected by PMC551. Write 1 to clear
31	Parity Error. Set to 1 in response to parity error. Write 1 to clear

5.1.2 BAR0

BAR0 is used to determine the size of the memory actually on the PMC551 in the system, and to assign the base PCI address of the region that the PMC551 will occupy.

Bit(s)	Function
0	0 - Indicates memory space address
1..2	Address range type. Not used by PMC551
3	Prefetch Enable. Set to enable prefetch. Should be set for best performance.
4..19	Reserved
20..31	Base Address

Memory sizing follows the PCI specification:

- Write all 1's to the register
- Read back

On the reading a mask is returned in which all address bits that are NOT decoded by the PMC551 are returned as set. (Example: on a PMC551 configured for 32Mbyte the return value will be: 0xFE000000).

Once the memory size is determined the base address value is set.

Note: On most systems, this function is automatically performed by the BIOS or other power on initialization. Care must be exercised when modifying this register. Prior to altering the value, ensure that the Memory Enable (bit 1 in the CMD/STS register) is zero.

5.2 Waking up Memory

After power up, prior to accessing the memory on the PMC551, a "wakeup" procedure must be executed. The following code fragment documents the necessary interactions. The procedures prefixed with "pci_" should be implemented or replaced as appropriate for the local software environment.

They perform 16 bit (word) or 32 bit (dword) PCI configuration transfers.

```
#define PMC551_SDRAM_MA       0x60
#define PMC551_SDRAM_CMD      0x62
#define PMC551_DRAM_CFG       0x64
#define PMC551_COMMAND_DONE   0x01
/*
 * Initialization for the PMC551
 * PCI device ID 0x020011b0
 */
void initPMC551 (struct pci_dev *dev) {
      int cmd;
      int i,k;

      pci_write_config_word( dev, PMC551_SDRAM_MA, 0x0400);
      pci_write_config_word( dev, PMC551_SDRAM_CMD, 0x00bf );

     do { pci_read_config_word( dev, PMC551_SDRAM_CMD, &cmd ); }
           while ( PMC551_COMMAND_DONE & cmd );

      for ( i = 1; i<=8 ; i++) {
           pci_write_config_word ( dev, PMC551_SDRAM_CMD, 0x0df );
           do { pci_read_config_word( dev, PMC551_SDRAM_CMD, &cmd ); }
                 while ( PMC551_COMMAND_DONE & cmd );
      }

      pci_write_config_word ( dev, PMC551_SDRAM_MA, 0x0020 );
      pci_write_config_word ( dev, PMC551_SDRAM_CMD, 0x0ff );

      do { pci_read_config_word ( dev, PMC551_SDRAM_CMD, &cmd ); }
           while ( PMC551_COMMAND_DONE & cmd );

      pci_read_config_dword ( dev, PMC551_DRAM_CFG, &k );
      k |= 0x02000000;
      pci_write_config_dword ( dev, PMC551_DRAM_CFG, k );
```

6 SPECIFICATIONS

6.1 General

General specifications for PMC551 are listed below.

CHARACTERISTICS	SPECIFICATIONS
DRAM Memory Subsystem	up to 512Mbyte
Compatibility	IEEE802.3z, Standard Single PMC
Interface: PCI 33Mhz 32bit	PCI Revision 2.2
Size	IEEE1386, Standard Single PMC
Drivers	VxWorks, pSOS, Lynx, Linux. (Contact **RAMiX** for additional software support information)
Temperature Operating Storage	 0°C to 65°C -40°C to 85°C
Power Requirements	+3.3V @ 1.5A (typical) +5V @ 0.3A (typical)